P4C1041
HIGH SPEED 256K x 16 (4 MEG) STATIC CMOS RAM

FEATURES

- **High Speed (Equal Access and Cycle Times)**
  - **— 10/12/15/20 ns (Commercial)**
  - **— 12/15/20 ns (Industrial/Military)**
- **Low Power**
- **Single 5.0V ± 10% Power Supply**
- **2.0V Data Retention**
- **Easy Memory Expansion Using $\overline{CE}$ and $\overline{OE}$ Inputs**
- **Fully TTL Compatible Inputs and Outputs**
- **Advanced CMOS Technology**
- **Fast t_{OE}**
- **Automatic Power Down when deselected**
- **Packages**
  - **—44-Pin SOJ, TSOP II**

DESCRIPTION

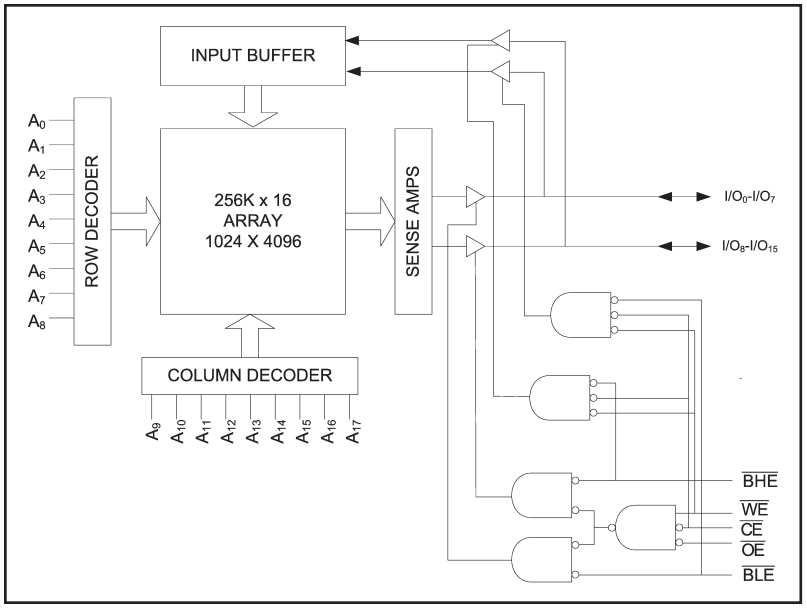
The P4C1041 is a 262,144 words by 16 bits high-speed CMOS static RAM. The CMOS memory requires no clocks or refreshing, and has equal access and cycle times. Inputs are fully TTL-compatible. The RAM operates from a single 5.0V ± 10% tolerance power supply.

Access times as fast as 10 nanoseconds permit greatly enhanced system operating speeds. CMOS is utilized to reduce power consumption to a low level. The P4C1041 is a member of a family of PACE RAM™ products offering fast access times.

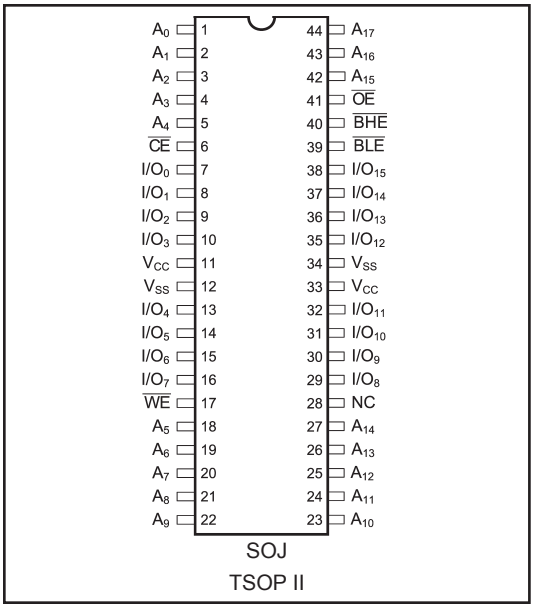
The P4C1041 device provides asynchronous operation with matching access and cycle times. Memory locations are specified on address pins A_0 to A_{17}. Reading is accomplished by device selection ($\overline{CE}$ and output enabling ($\overline{OE}$) while write enable ($\overline{WE}$) remains HIGH. By presenting the address under these conditions, the data in the addressed memory location is presented on the data input/output pins. The input/output pins stay in the HIGH Z state when either $\overline{CE}$ or $\overline{OE}$ is HIGH or $\overline{WE}$ is LOW.

Package options for the P4C1041 include 44-pin SOJ and TSOP packages.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



SOJ
TSOP II

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade[2]	Ambient Temperature	GND	V_{CC}
Commercial	0 - 70°C	0V	5.0V ± 10%
Industrial	-40 - 85°C	0V	5.0V ± 10%
Military	-55 - 125°C	0V	5.0V ± 10%

CAPACITANCES [4]

V_{CC} = 5.0V, T_A = 25°C, f = 1.0MHz

Sym	Parameter	Conditions	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

MAXIMUM RATINGS [1]

Sym	Parameter	Value	Unit
V_{CC}	Power Supply Pin with Respect to GND	-0.5 to 7.0	V
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to VCC+0.5	V
T_A	Operating Temperature	-55 to 125	°C
T_{BIAS}	Temperature Under Bias	-55 to 125	°C
T_{STG}	Storage Temperature	-65 to 150	°C
I_{OUT}	DC Output Current	20	mA

DC ELECTRICAL CHARACTERISTICS

Over recommended operating temperature and supply voltage [2]

Sym	Parameter	Test Conditions	P4C1041		Unit
			Min	Max	
V_{IH}	Input High Voltage		2.2	V_{CC} +0.5	V
V_{IL}	Input Low Voltage		-0.5[3]	0.8	V
V_{OL}	Output Low Voltage (TTL Load)	I_{OL} = +8 mA, V_{CC} = Min.		0.4	V
V_{OH}	Output High Voltage (TTL Load)	I_{OH} = –4 mA, V_{CC} = Min.	2.4		V
I_{LI}	Input Leakage Current	V_{CC} = Max. V_{IN} = GND to V_{CC}	-2	+2	µA
I_{LO}	Output Leakage Current	V_{CC} = Max., $\overline{CE}$ = V_{IH}, V_{OUT} = GND to V_{CC}	-1	+1	µA
I_{SB}	Standby Power Supply Current (TTL Input Levels)	$\overline{CE} \geq V_{IH}$ V_{CC}= Max, f = Max., Outputs Open $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$	—	40	mA
I_{SB1}	Standby Power Supply Current (CMOS Input Levels)	$\overline{CE} \geq V_{CC}$ - 0.2V V_{CC}= Max, f = 0, Outputs Open $V_{IN} \geq V_{CC}$ - 0.3V or $V_{IN} \leq$ 0.3V	—	6	mA

POWER DISSIPATION CHARACTERISTICS VS. SPEED

Sym	Parameter	Temperature Range	-10	-12	-15	-20	Unit
I_{CC}	Dynamic Operating Current*	Commercial	100	90	80	70	mA
		Industrial	100	90	80	70	mA
		Military	N/A	110	100	90	mA

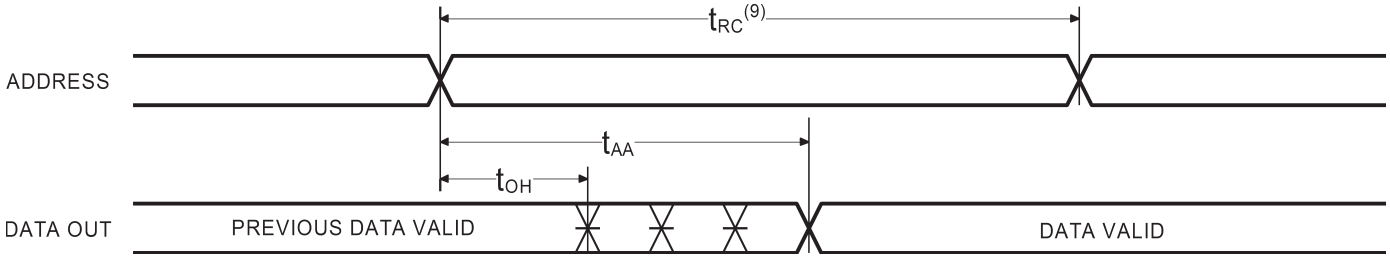
*V_{CC} = 3.6V. Tested with outputs open. f = Max. Switching inputs are 0V and 3V. $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}.

AC ELECTRICAL CHARACTERISTICS—READ CYCLE

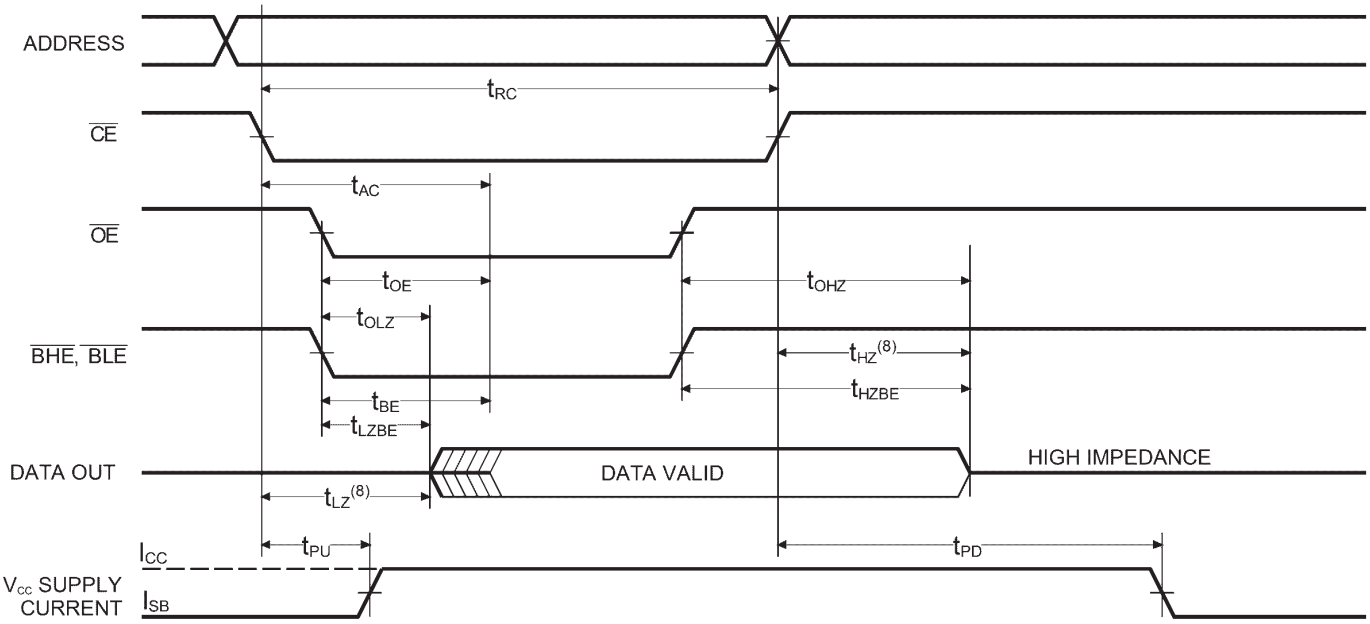
(V_{CC} = 5.0V ± 10%, All Temperature Ranges) [2]

Sym	Parameter	-10		-12		-15		-20		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{RC}	Read Cycle Time	10		12		15		20		ns
t_{AA}	Address Access Time		10		12		15		20	ns
t_{AC}	Chip Enable Access Time		10		12		15		20	ns
t_{OH}	Output Hold from Address Change	3		3		3		3		ns
t_{LZ}	Chip Enable to Output in Low Z	3		3		3		3		ns
t_{HZ}	Chip Disable to Output in High Z		5		6		7		8	ns
t_{OE}	Output Enable Low to Data Valid		5		6		7		8	ns
t_{OLZ}	Output Enable Low to Low Z	0		0		0		0		ns
t_{OHZ}	Output Enable High to High Z		5		6		7		8	ns
t_{PU}	Chip Enable to Power Up Time	0		0		0		0		ns
t_{PD}	Chip Disable to Power Down Time		10		12		15		20	ns
t_{BE}	Byte Enable to Data Valid		5		6		7		8	ns
t_{LZBE}	Byte Enable to Low Z	0		0		0		0		ns
t_{HZBE}	Byte Disable to High Z		6		6		7		8	ns

TIMING WAVEFORM OF READ CYCLE NO. 1



TIMING WAVEFORM OF READ CYCLE NO. 2 ($\overline{OE}$ CONTROLLED)(5,6)



Notes:

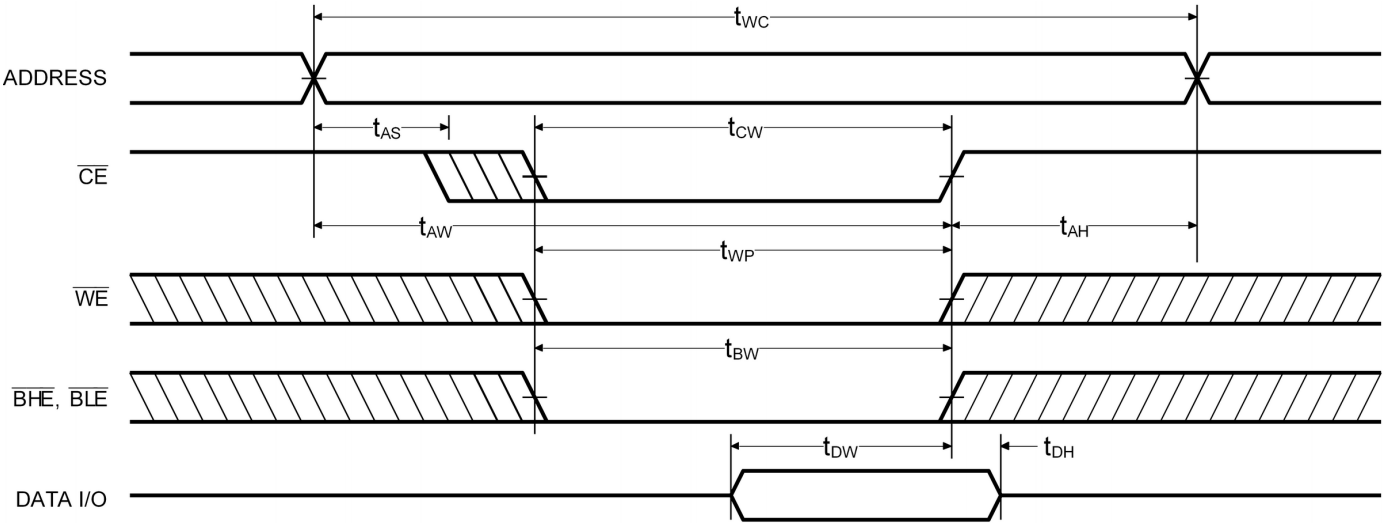
1. Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to MAXIMUM rating conditions for extended periods may affect reliability.
2. Extended temperature operation guaranteed with 400 linear feet per minute of air flow.
3. Transient inputs with V_{IL} not more negative than –2.0V and $V_{IH} \leq V_{CC}$ + 0.5V, are permissible for pulse widths up to 20 ns.
4. This parameter is sampled and not 100% tested.
5. $\overline{WE}$ is HIGH for READ cycle.
6. $\overline{CE}$ is LOW and $\overline{OE}$ is LOW for READ cycle.
7. ADDRESS must be valid prior to, or coincident with $\overline{CE}$ transition LOW.
8. Transition is measured ± 200 mV from steady state voltage prior to change, with loading as specified in Figure 1. This parameter is sampled and not 100% tested.
9. Read Cycle Time is measured from the last valid address to the first transitioning address.

AC CHARACTERISTICS—WRITE CYCLE

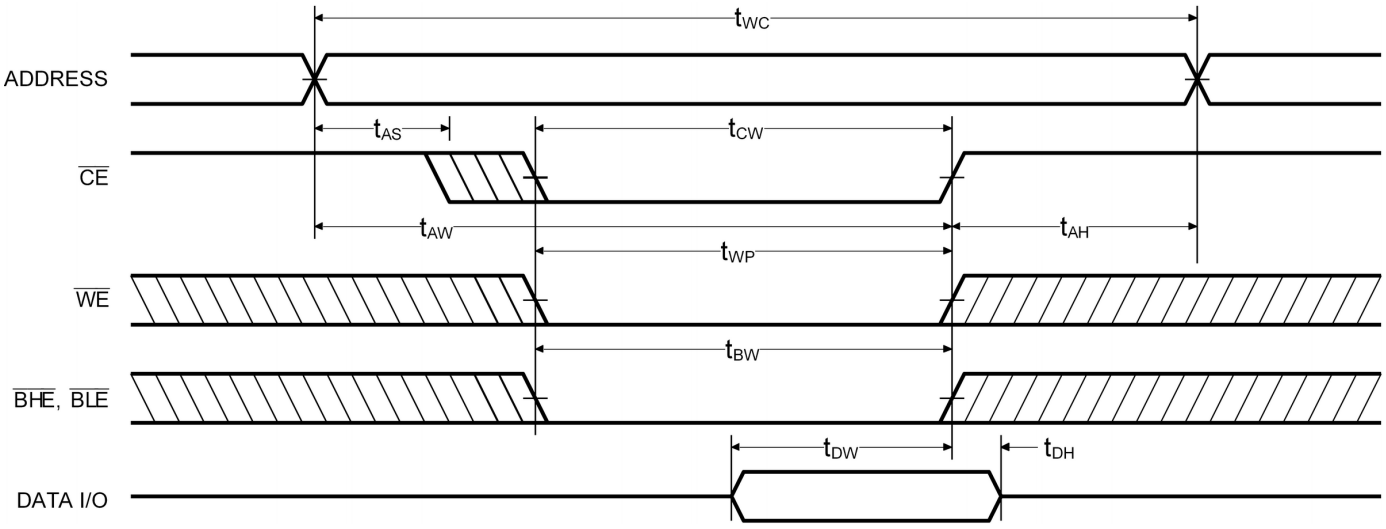
(V_{CC} = 5.0V ± 10%, All Temperature Ranges)[2]

Sym.	Parameter	-10		-12		-15		-20		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{WC}	Write Cycle Time	10		12		15		20		ns
t_{CW}	Chip Enable Time To End Of Write	7		8		10		10		ns
t_{AW}	Address Valid To End Of Write	7		8		10		10		ns
t_{AS}	Address Setup Time To Write Start	0		0		0		0		ns
t_{WP}	Write Pulse Width	7		8		10		10		ns
t_{AH}	Address Hold Time	0		0		0		0		ns
t_{DW}	Data Valid To End Of Write	5		6		7		8		ns
t_{DH}	Data Hold Time	0		0		0		0		ns
t_{WZ}	Write Enable To Output In High Z		5		6		7		8	ns
t_{OW}	Output Active From End Of Write	5		5		0		0		ns
t_{LZWE}	$\overline{WE}$ High To Low Z	3		3		3		3		ns
t_{BW}	Byte Enable To End Of Write	7		8		10		10		ns

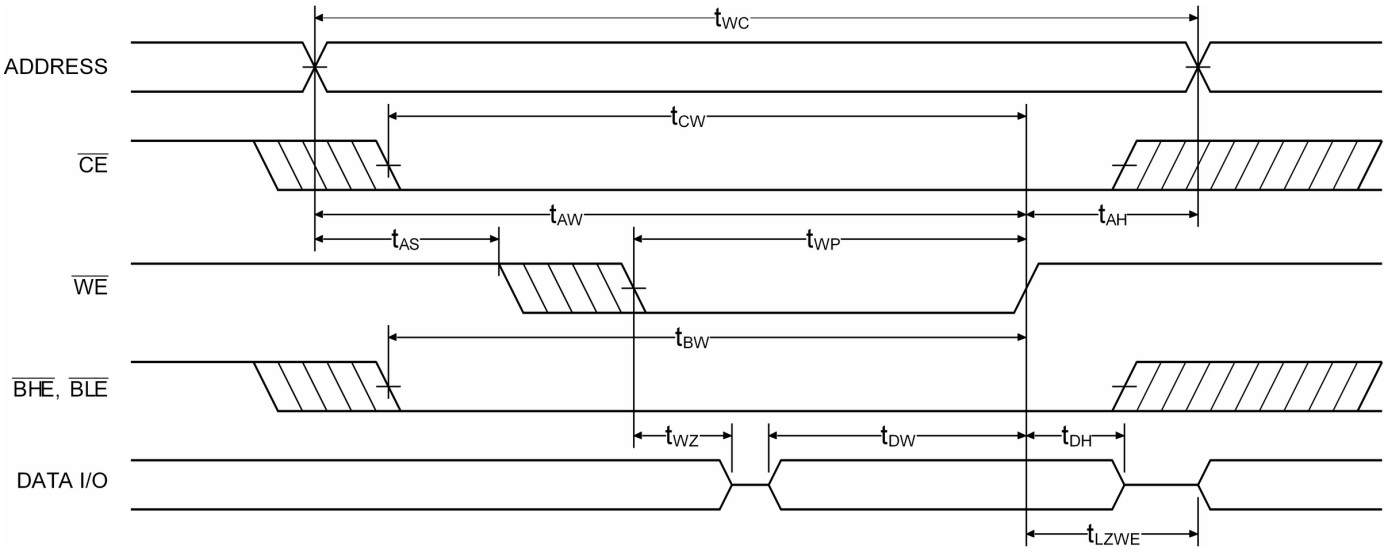
TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{CE}$ CONTROLLED)



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{BLE}$ OR $\overline{BHE}$ CONTROLLED)



TIMING WAVEFORM OF WRITE CYCLE NO. 3 ($\overline{WE}$ CONTROLLED, $\overline{OE}$ LOW)



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns
Input Timing Reference Level	1.5V
Output Timing Reference Value	1.5V
Output Load	See Figures 1 & 2

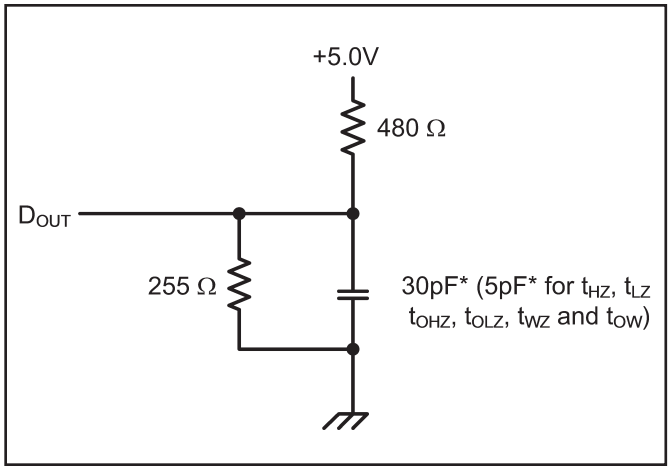


Figure 1. Output Load

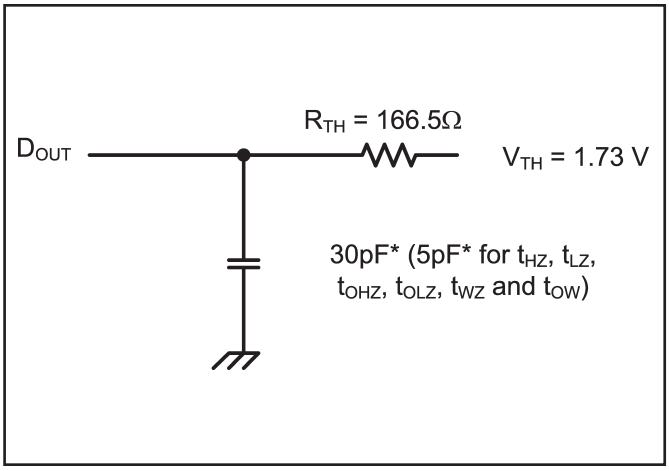


Figure 2. Thevenin Equivalent

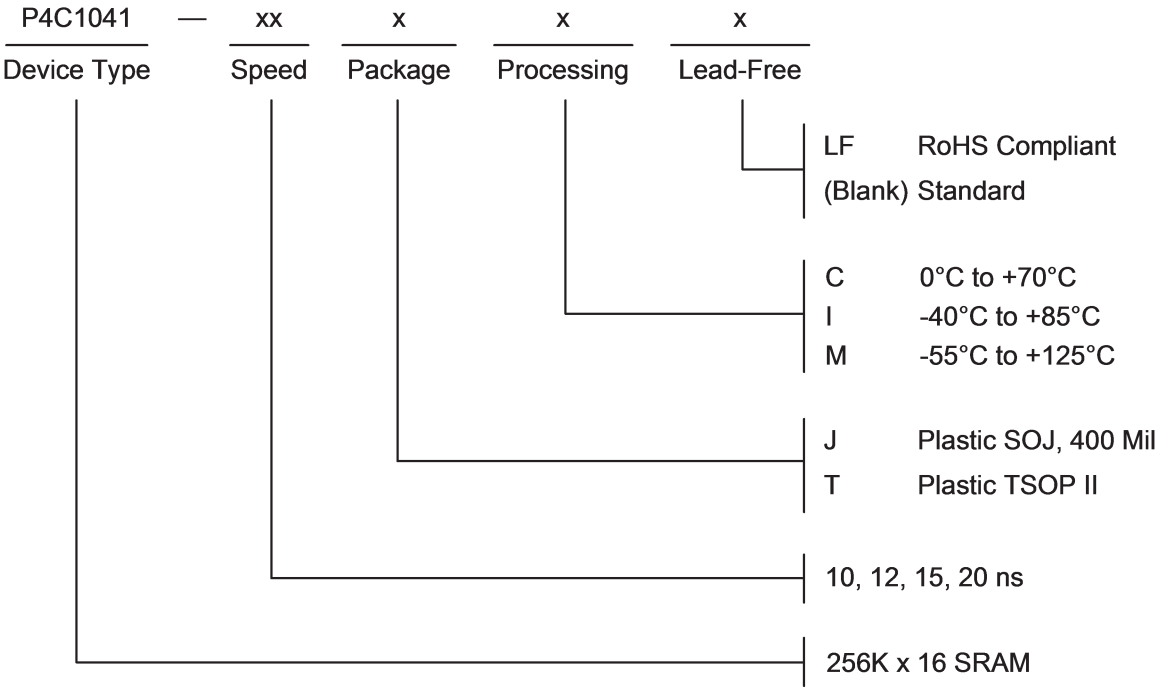
* including scope and test fixture.

Note:
Because of the ultra-high speed of the P4C1041, care must be taken when testing this device; an inadequate setup can cause a normal functioning part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the V_{CC} and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between V_{CC} and ground. To avoid signal reflections, proper termination must be used; for example, a 50Ω test environment should be terminated into a 50Ω load with 1.73V (Thevenin Voltage) at the comparator input, and a 116Ω resistor must be used in series with D_{OUT} to match 166Ω (Thevenin Resistance).

TRUTH TABLE

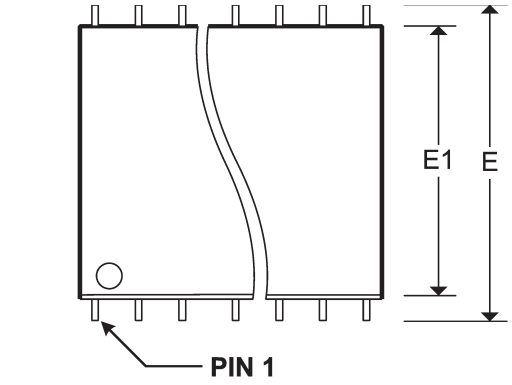
Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	I/O_0 - I/O_7	I/O_8 - I/O_{15}	Power
Powerdown	H	X	X	X	X	High Z	High Z	Standby
Read All Bits	L	L	H	L	L	D_{OUT}	D_{OUT}	Active
Read Lower Bits Only	L	L	H	L	H	D_{OUT}	High Z	Active
Read Upper Bits Only	L	L	H	H	L	High Z	D_{OUT}	Active
Write All Bits	L	X	L	L	L	D_{IN}	D_{IN}	Active
Write Lower Bits Only	L	X	L	L	H	D_{IN}	High Z	Active
Write Upper Bits Only	L	X	L	H	L	High Z	D_{IN}	Active
Selected, Outputs Disabled	L	H	H	X	X	High Z	High Z	Active

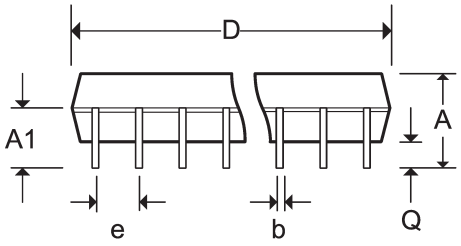
ORDERING INFORMATION

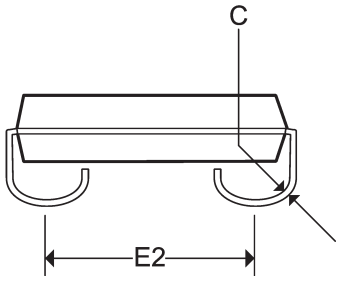


Pkg #	J8	
# Pins	44 (400 mil)	
Symbol	**Min**	**Max**
A	0.128	0.148
A1	0.082	-
b	0.013	0.023
C	0.007	0.013
D	1.120	1.130
e	0.050 BSC	
E	0.435	0.445
E1	0.395	0.405
E2	0.370 BSC	
Q	0.025	-

SOJ SMALL OUTLINE IC PACKAGE

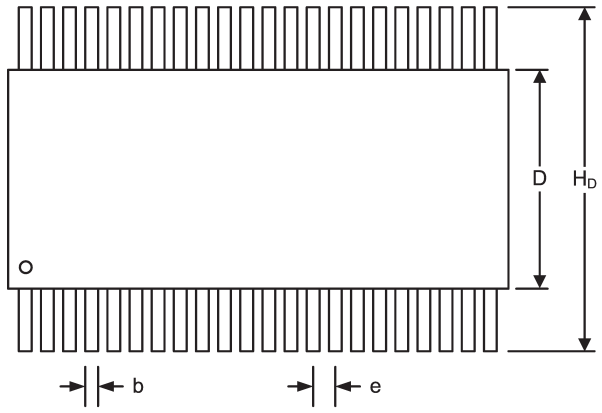


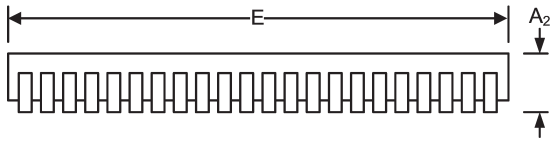


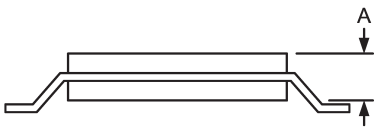


Pkg #	T2	
# Pins	44	
Symbol	**Min**	**Max**
A	0.039	0.047
A_2	0.033	0.045
b	0.012	0.016
D	0.396	0.404
E	0.721	0.729
e	0.0315 BSC	
H_D	0.462	0.470

TSOP II THIN SMALL OUTLINE PACKAGE







REVISIONS

DOCUMENT NUMBER	SRAM 133
DOCUMENT TITLE	P4C1041 HIGH SPEED 256K X 16 (4 MEG) STATIC CMOS RAM

REV	ISSUE DATE	ORIGINATOR	DESCRIPTION OF CHANGE
OR	Jan-2007	JDB	New Data Sheet
A	July-2008	JDB	Added Military processing, lead-free designation
B	Sept-2009	JDB	Updated TSOP II Package Drawing