PYRAMID
SEMICONDUCTOR CORPORATION

P4C107

ULTRA HIGH SPEED 1M X 1 STATIC CMOS RAM

FEATURES

- **Full CMOS**
- **High Speed (Equal Access and Cycle Times)**
  - **– 10/12/15 ns (Commercial)**
  - **– 12/15/20 ns (Industrial)**
- **Single 5V±10% Power Supply**
- **Separate Data I/O**
- **Three-State Output**
- **Fully TTL Compatible Inputs and Outputs**
- **Standard Pinout (JEDEC Approved)**
  - **– 28-Pin 400 mil SOJ**

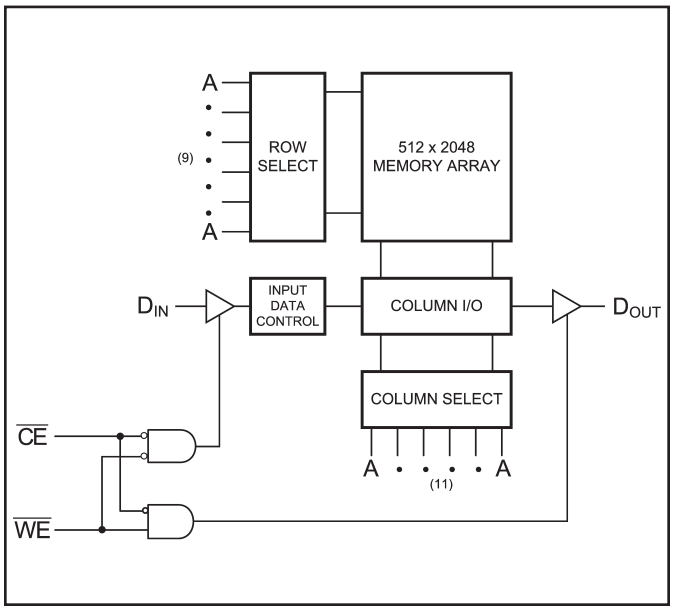
DESCRIPTION

The P4C107 is a 1Mx1-bit ultra high-speed static RAM. The CMOS memories require no clocks or refreshing and have equal access and cycle times. The RAM operates from a single 5V ± 10% tolerance power supply. Data integrity is maintained for supply voltages down to 2.0V, typically drawing 50µA.

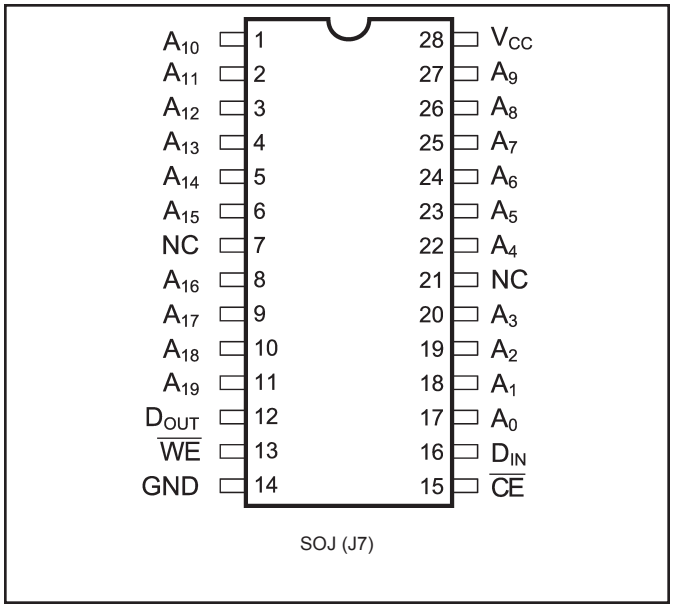
Access times as fast as 10 nanoseconds are available, greatly enhancing system speeds.

The P4C107 is available in a 28-pin 400 mil SOJ.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



SOJ (J7)

MAXIMUM RATINGS[1]

Sym	Parameter	Value	Unit
V_{CC}	Power Supply Pin with Respect to GND	-0.5 to +6	V
V_{TERM}	Terminal Voltage with Respect to GND (up to 6.0V)	-0.5 to V_{CC} + 0.5	V
T_A	Operating Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

RECOMMENDED OPERATING CONDITIONS

Grade[2]	Ambient Temp	GND	V_{CC}
Commercial	0°C to +70°C	0V	5.0V ± 10%
Industrial	-40°C to +85°C	0V	5.0V ± 10%

CAPACITANCES[4]

(V_{CC} = 5.0V, T_A = 25°C, f = 1.0MHz)

Sym	Parameter	Conditions	Typ	Unit
C_{IN}	Input Capacitance	V_{IN}=0V	7	pF
C_{OUT}	Output Capacitance	V_{OUT}=0V	10	pF

DC ELECTRICAL CHARACTERISTICS

(Over Recommended Operating Temperature & Supply Voltage)[2]

Sym	Parameter	Test Conditions	Min	Max	Unit
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.5	V
V_{IL}	Input Low Voltage		-0.5[3]	0.8	V
V_{OL}	Output Low Voltage (TTL Load)	I_{OL} = +8 mA, V_{CC} = Min		0.4	V
V_{OH}	Output High Voltage (TTL Load)	I_{OH} = -4 mA, V_{CC} = Min	2.4		V
I_{LI}	Input Leakage Current	V_{CC} = Max, V_{IN} = GND to V_{CC}	-5	+5	µA
I_{LO}	Output Leakage Current	V_{CC} = Max, $\overline{CE}$ = V_{IH}, V_{OUT} = GND to V_{CC}	-5	+5	µA
I_{CC}	Operating Supply Current	V_{CC} = Max, I_{OUT}=0 mA, f=Max		150	mA
I_{SB}	Standby Power Supply Current (TTL Input Levels)	$\overline{CE}$ ≥ V_{IH}, V_{CC} = Max, f = Max, Outputs Open		50	mA
I_{SB1}	Standby Power Supply Current (CMOS Input Levels)	$\overline{CE}$ ≥ V_{HC}, V_{CC} = Max, f = 0, Outputs Open V_{IN} ≤ V_{LC} or V_{IN} ≥ V_{HC}		3	mA

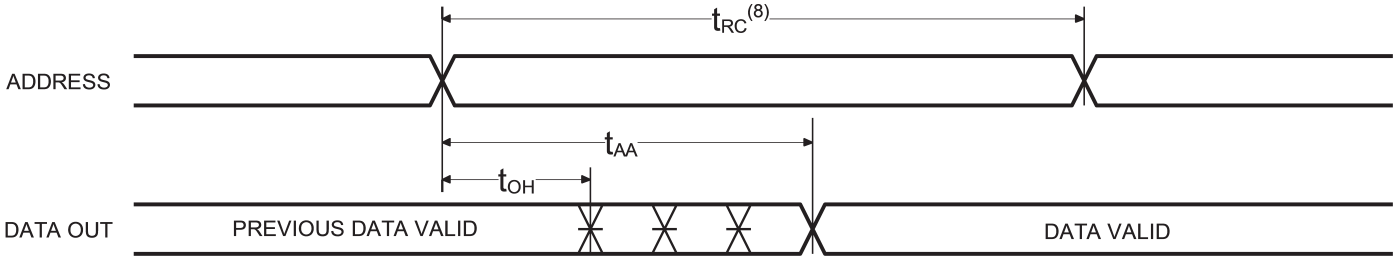
N/A = Not applicable

AC ELECTRICAL CHARACTERISTICS—READ CYCLE

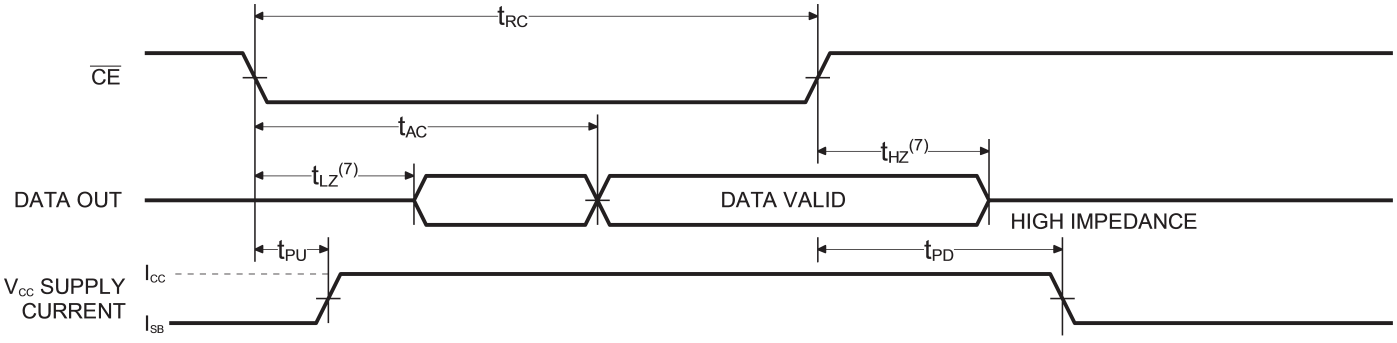
(V_{CC} = 5V ± 10%, All Temperature Ranges)[2]

Sym	Parameter	-10		-12		-15		-20		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{RC}	Read Cycle Time	10		12		15		20		ns
t_{AA}	Address Access Time		10		12		15		20	ns
t_{AC}	Chip Enable Access Time		10		12		15		20	ns
t_{OH}	Output Hold from Address Change	3		3		3		3		ns
t_{LZ}	Chip Enable to Output in Low Z	3		3		3		3		ns
t_{HZ}	Chip Disable to Output in High Z		5		6		7		8	ns
t_{PU}	Chip Enable to Power Up Time	0		0		0		0		ns
t_{PD}	Chip Disable to Power Down		10		12		15		20	ns

TIMING WAVEFORM OF READ CYCLE NO. 1 (ADDRESS CONTROLLED)[5,6]



TIMING WAVEFORM OF READ CYCLE NO. 2 ($\overline{CE}$ CONTROLLED)[5,7,8]

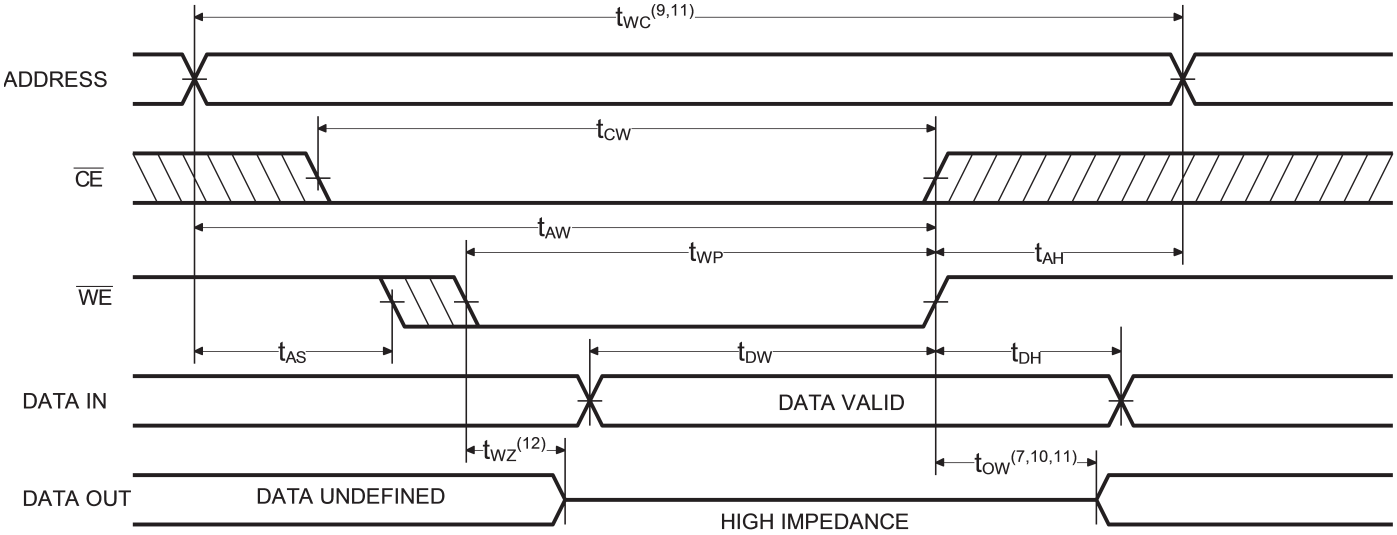


AC CHARACTERISTICS—WRITE CYCLE

(V_{CC} = 5V ± 10%, All Temperature Ranges)[2]

Sym	Parameter	-10		-12		-15		-20		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{WC}	Write Cycle Time	10		12		15		20		ns
t_{CW}	Chip Enable Time to End of Write	7		10		12		15		ns
t_{AW}	Address Valid to End of Write	7		10		12		15		ns
t_{AS}	Address Setup Time	0		0		0		0		ns
t_{WP}	Write Pulse Width	7		10		12		15		ns
t_{AH}	Address Hold Time	0		0		0		0		ns
t_{DW}	Data Valid to End of Write	6		7		8		10		ns
t_{DH}	Data Hold Time	0		0		0		0		ns
t_{WZ}	Write Enable to Output in High Z		6		7		8		9	ns
t_{OW}	Output Active from End of Write	0		0		0		0		ns

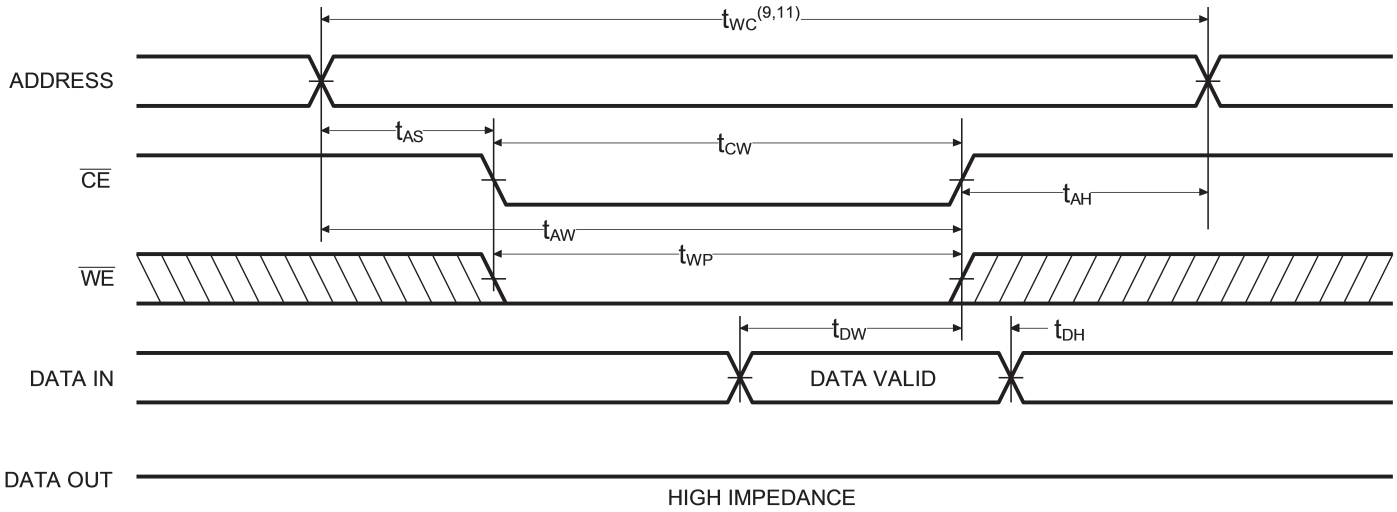
TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)[10,11]



Notes:

1. Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to MAXIMUM rating conditions for extended periods may affect reliability.
2. Extended temperature operation guaranteed with 400 linear feet per minute of air flow.
3. Transient inputs with V_{IL} and I_{IL} not more negative than –3.0V and –100mA, respectively, are permissible for pulse widths up to 20ns.
4. This parameter is sampled and not 100% tested.
5. $\overline{WE}$ is HIGH for READ cycle.
6. $\overline{CE}$ is LOW and $\overline{OE}$ is LOW for READ cycle.
7. ADDRESS must be valid prior to, or coincident with $\overline{CE}$ transition LOW.
8. Transition is measured ± 200 mV from steady state voltage prior to change, with loading as specified in Figure 1. This parameter is sampled and not 100% tested.
9. Read Cycle Time is measured from the last valid address to the first transitioning address.

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CE}$ CONTROLLED)[10]



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns
Input Timing Reference Level	1.5V
Output Timing Reference Level	1.5V
Output Load	See Figures 1 and 2

TRUTH TABLE

Mode	$\overline{CE}$	$\overline{WE}$	I/O	Power
Standby	H	X	High Z	Standby
Read	L	H	D_{OUT}	Active
Write	L	L	High Z	Active

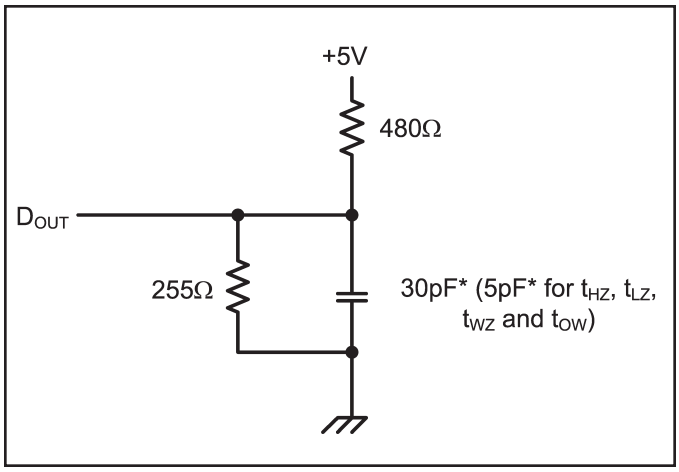


Figure 1. Output Load

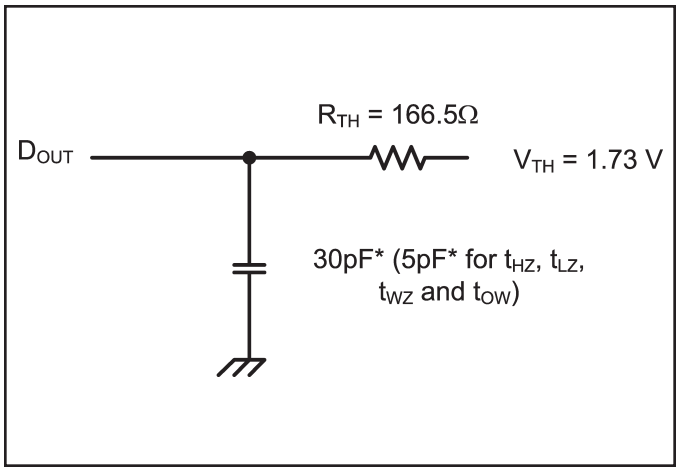


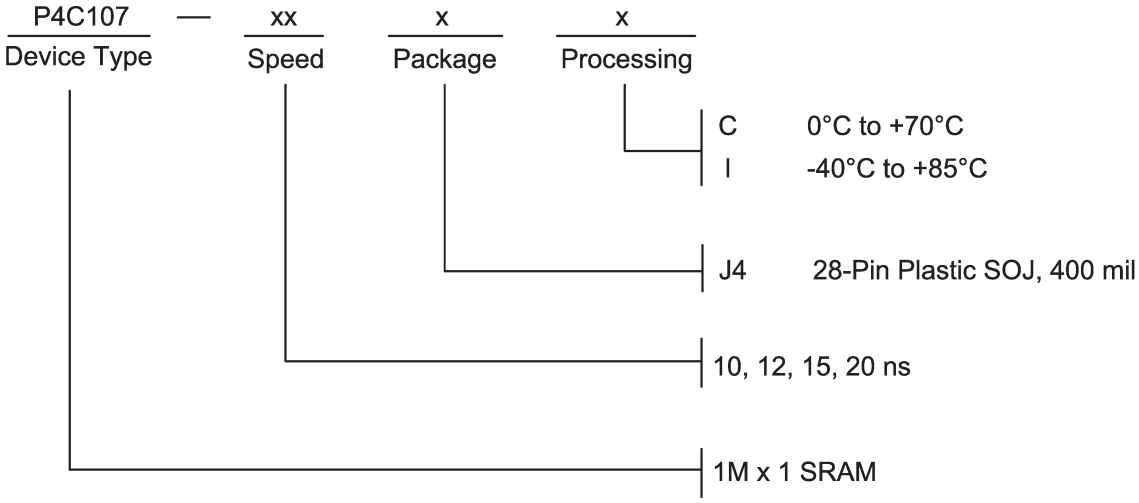
Figure 2. Thevenin Equivalent

* including scope and test fixture.

Note:
Because of the ultra-high speed of the P4C107, care must be taken when testing this device; an inadequate setup can cause a normal functioning part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the V_{CC} and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between V_{CC} and ground. To avoid signal reflections, proper termination must be used; for example, a 50Ω test environment should be terminated into a 50Ω load with 1.73V (Thevenin Voltage) at the comparator input, and a 116Ω resistor must be used in series with D_{OUT} to match 166Ω (Thevenin Resistance).

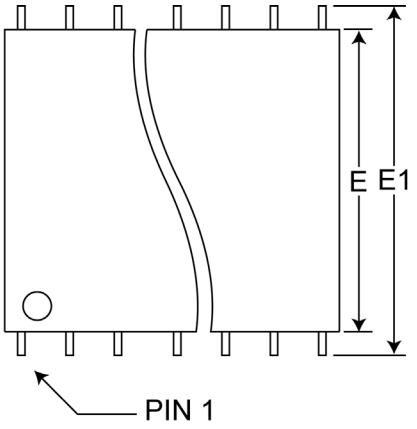
Notes:
10. $\overline{CE}$ and $\overline{WE}$ must be LOW for WRITE cycle.
11. $\overline{OE}$ is LOW for this WRITE cycle to show t_{WZ} and t_{OW}.
12. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high impedance state
13. Write Cycle Time is measured from the last valid address to the first transitioning address.

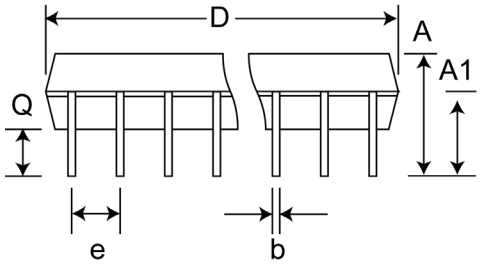
ORDERING INFORMATION

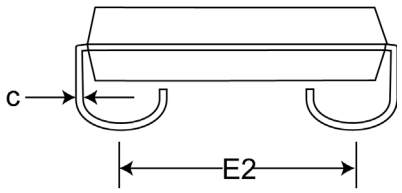


Pkg #	J7	
# Pins	28 (400 mil)	
Symbol	**Min**	**Max**
A	0.128	0.148
A1	0.082	-
b	0.013	0.019
C	0.007	0.013
D	0.720	0.730
e	0.050 BSC	
E	0.395	0.405
E1	0.435	0.445
E2	0.360	0.380
Q	0.025	-

SOJ SMALL OUTLINE IC PACKAGE







REVISIONS

DOCUMENT NUMBER	SRAM139
DOCUMENT TITLE	P4C107 - ULTRA HIGH SPEED 1M X 1 STATIC CMOS RAM

REV	ISSUE DATE	ORIGINATOR	DESCRIPTION OF CHANGE
OR	Apr-2010	JDB	New Data Sheet