PYRAMID
SEMICONDUCTOR CORPORATION

PYA28C256

32K X 8 EEPROM

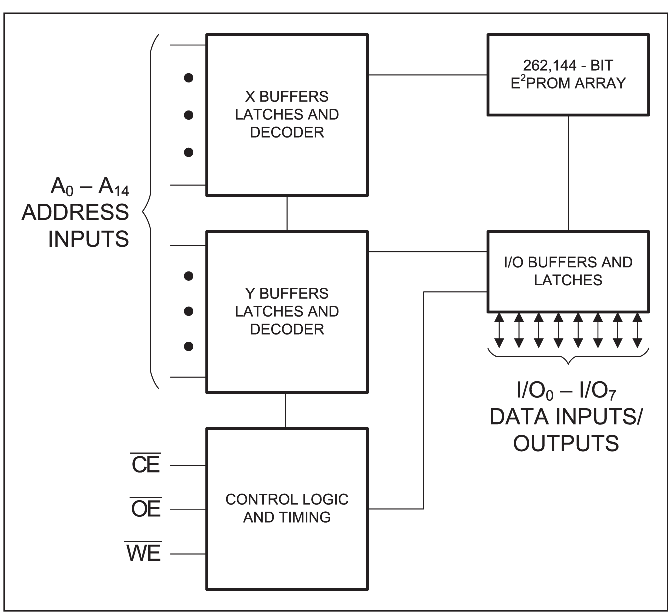
FEATURES

- Access Times of 150, 200, 250 and 350ns
- Single 5V±10% Power Supply
- Simple Byte and Page Write
- Low Power CMOS:
  - 60 mA Active Current
  - 300 µA Standby Current
- Fast Write Cycle Times
- Software Data Protection
- CMOS & TTL Compatible Inputs and Outputs
- Endurance:
  - 10,000 Write Cycles
  - 100,000 Write Cycles (optional)
- Data Retention: 10 Years
- Available in the following package:
  – 28-Pin 600 mil Ceramic DIP
  – 32-Pin Ceramic LCC (450x550 mils)

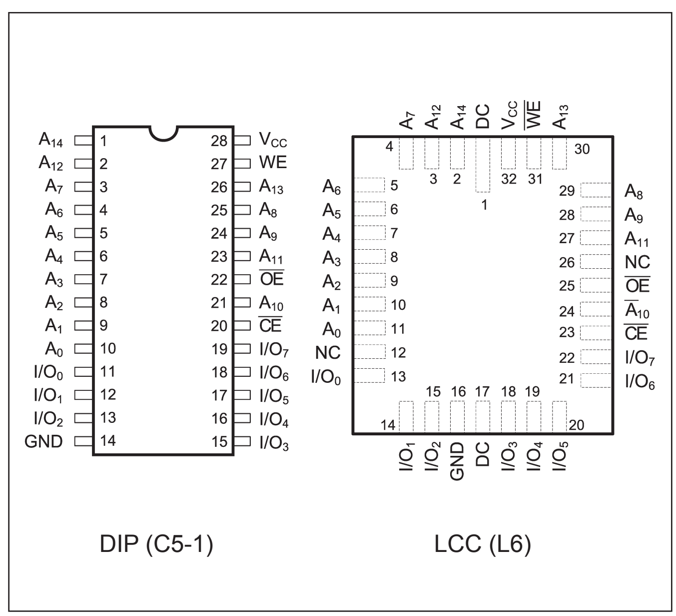
DESCRIPTION

The PYA28C256 is a 5 Volt 32Kx8 EEPROM. The device supports 64-byte page write operation. The PYA28C256 features $\overline{\text{DATA}}$ and Toggle Bit Polling as well as a system software scheme used to indicate early completion of a Write Cycle. The device also includes user-optional software data protection. Data Retention is 10 Years. The device is available in a 28-Pin 600 mil wide Ceramic DIP and 32-Pin LCC.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



OPERATION

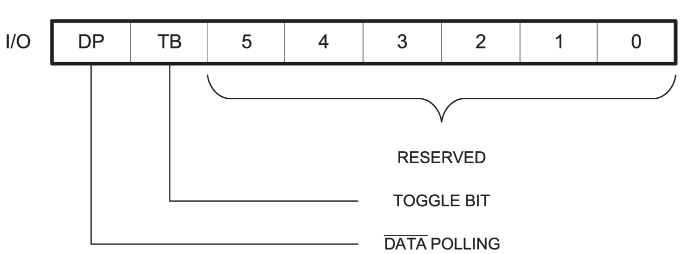
READ
Read operations are initiated by both $\overline{OE}$ and $\overline{CE}$ LOW. The read operation is terminated by either $\overline{CE}$ or $\overline{OE}$ returning HIGH. This two line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either $\overline{OE}$ or $\overline{CE}$ is HIGH.

BYTE WRITE
Write operations are initiated when both $\overline{CE}$ and $\overline{WE}$ are LOW and $\overline{OE}$ is HIGH. The PYA28C256 supports both a $\overline{CE}$ and $\overline{WE}$ controlled write cycle. That is, the address is latched by the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs last. Similarly, the data is latched internally by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs first. A byte write operation, once initiated, will automatically continue to completion.

PAGE WRITE
The page write feature of the PYA28C256 allows 1 to 64 bytes of data to be consecutively written to the PYA28C256 during a single internal programming cycle. The host can fetch data from another device within the system during a page write operation (change the source address), but the page address (A_6 through A_{14}) for each subsequent valid write cycle to the part during this operation must be the same as the initial page address. The bytes within the page to be written are specified with the A_0 through A_5 inputs.

The page write mode can be initiated during any write operation. Following the initial byte write cycle, the host can write an additional 1 to 63 bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the $\overline{WE}$ HIGH to LOW transition, must begin within 150µs of the falling edge of the preceding $\overline{WE}$. If a subsequent $\overline{WE}$ HIGH to LOW transition is not detected within 150µs, the internal automatic programming cycle will commence. There is no page write window limitation. Effectively, the page write window is infinitely wide, so long as the host continues to access the device within the byte load cycle time of 150µs.

WRITE STATUS BITS
The PYA28C256 provides the user two write operation status bits. These can be used to optimize a system write cycle time. The status bits are mapped onto the I/O bus as shown below.



DATA POLLING
The PYA28C256 features $\overline{DATA}$ Polling as a method to indicate to the host system that the byte write or page write cycle has completed. $\overline{DATA}$ Polling allows a simple bit test operation to determine the status of the PYA28C256, eliminating additional interrupts or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O_7 (i.e., write data=0xxx xxxx, read data=1xxx xxxx). Once the programming cycle is complete, I/O_7 will reflect true data. Note: If the PYA28C256 is in the protected state and an illegal write operation is attempted, $\overline{DATA}$ Polling will not operate.

TOGGLE BIT
The PYA28C256 also provides another method for determining when the internal write cycle is complete. During the internal programming cycle, I/O_6 will toggle from HIGH to LOW and LOW to HIGH on subsequent attempts to read the device. When the internal cycle is complete the toggling will cease and the device will be accessible for addtional read or write operations.

DATA PROTECTION
Pyramid has incorporated both hardware and software features that will protect the memory against inadvertent writes during transitions of the host system power supply.

Hardware Protection
Hardware features protect against inadvertent writes to the PYA28C256 in the following ways: (a) VCC sense - if VCC is below 3.8V (typical) the write function is inhibited; (b) VCC power-on delay - once VCC has reached 3.8V the device will automatically time out 5 ms (typical) before allowing a write; (c) write inhibit - holding any one of OE low, CE high or WE high inhibits write cycles; and (d) noise filter - pulses of less than 15 ns (typical) on the WE or CE inputs will not initiate a write cycle.

Software Data Protection
A software controlled data protection feature has been implemented on the PYA28C256. When enabled, the software data protection (SDP), will prevent inadvertent writes. The SDP feature may be enabled or disabled by the user; the PYA28C256 is shipped from Pyramid with SDP disabled.

SDP is enabled by the host system issuing a series of three write commands; three specific bytes of data are written to the three specific addresses (refer to "Software Data Protection" algorithm). After writing the 3-byte command sequence and after tWC the entire PYA28C256 will be protected against inadvertent write operations. It should be noted, that once protected the host may still perform a byte or page write to the PYA28C256. This is done by preceding the data to be written by the same

3-byte command sequence used to enable SDP.

Once set, SDP will remain active unless the disable command sequence is issued. Power transitions do not disable SDP and SDP will protect the PYA28C256 during power-up and power-down conditions. All command sequences must conform to the page write timing specifications. The data in the enable and disable command sequences is not written to the device and the memory addresses used in the sequence may be written with data in either a byte or page write operation.

After setting SDP, any attempt to write to the device without the 3-byte command sequence will start the internal write timers. No data will be written to the device; however, for the duration of tWC, read operations will effectively be polling operations.

DEVICE IDENTIFICATION

An extra 64 bytes of EEPROM memory are available to the user for device identification. By raising A9 to 12V ± 0.5V and using address locations 7FC0H to 7FFFH the additional bytes may be written to or read from in the same manner as the regular memory array.

OPTIONAL CHIP ERASE MODE

The entire device can be erased using a 6-byte software code. Please see "Software Chip Erase" application note at the end of this datasheet for details.

MAXIMUM RATINGS[1]

Sym	Parameter	Value	Unit
V_{CC}	Power Supply Pin with Respect to GND	-0.3 to +6.25	V
V_{TERM}	Terminal Voltage with Respect to GND (up to 6.25V)	-0.5 to +6.25	V
T_A	Operating Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

RECOMMENDED OPERATING CONDITIONS

Grade[2]	Ambient Temp	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%

CAPACITANCES[4]

(V_{CC} = 5.0V, T_A = 25°C, f = 1.0MHz)

Sym	Parameter	Conditions	Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	10	pF

DC ELECTRICAL CHARACTERISTICS

(Over Recommended Operating Temperature & Supply Voltage)[2]

Sym	Parameter	Test Conditions	PYA28C256		Unit
			Min	Max	
V_{IH}	Input High Voltage		2.0	V_{CC} + 0.3	V
V_{IL}	Input Low Voltage		-0.5[3]	0.8	V
V_{HC}	CMOS Input High Voltage		V_{CC} - 0.2	V_{CC} + 0.5	V
V_{LC}	CMOS Input Low Voltage		-0.5[3]	0.2	V
V_{OL}	Output Low Voltage (TTL Load)	I_{OL} = +2.1 mA, V_{CC} = Min		0.45	V
V_{OH}	Output High Voltage (TTL Load)	I_{OH} = -0.4 mA, V_{CC} = Min	2.4		V
I_{LI}	Input Leakage Current	V_{CC} = Max V_{IN} = GND to V_{CC}	-10	+10	µA
I_{LO}	Output Leakage Current	V_{CC} = Max, $\overline{CE}$ = V_{IH}, V_{OUT} = GND to V_{CC}	-10	+10	µA
I_{SB}	Standby Power Supply Current (TTL Input Levels)	$\overline{CE}$ ≥ V_{IH}, $\overline{OE}$ = V_{IL}, V_{CC} = Max, f = Max, Outputs Open	—	3	mA
I_{SB1}	Standby Power Supply Current (CMOS Input Levels)	$\overline{CE}$ ≥ V_{HC}, V_{CC} = Max, f = 0, Outputs Open, V_{IN} ≤ V_{LC} or V_{IN} ≥ V_{HC}	—	300	µA
I_{CC}	Supply Current	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}, All I/O's = Open, Inputs = V_{CC} = 5.5V	—	60	mA

Notes:

1. Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to MAXIMUM rating conditions for extended periods may affect reliability.
2. Extended temperature operation guaranteed with 400 linear feet per minute of air flow.
3. Transient inputs with V_{IL} and I_{IL} not more negative than -3.0V and -100mA, respectively, are permissible for pulse widths up to 20ns.
4. This parameter is sampled and not 100% tested.

POWER-UP TIMING

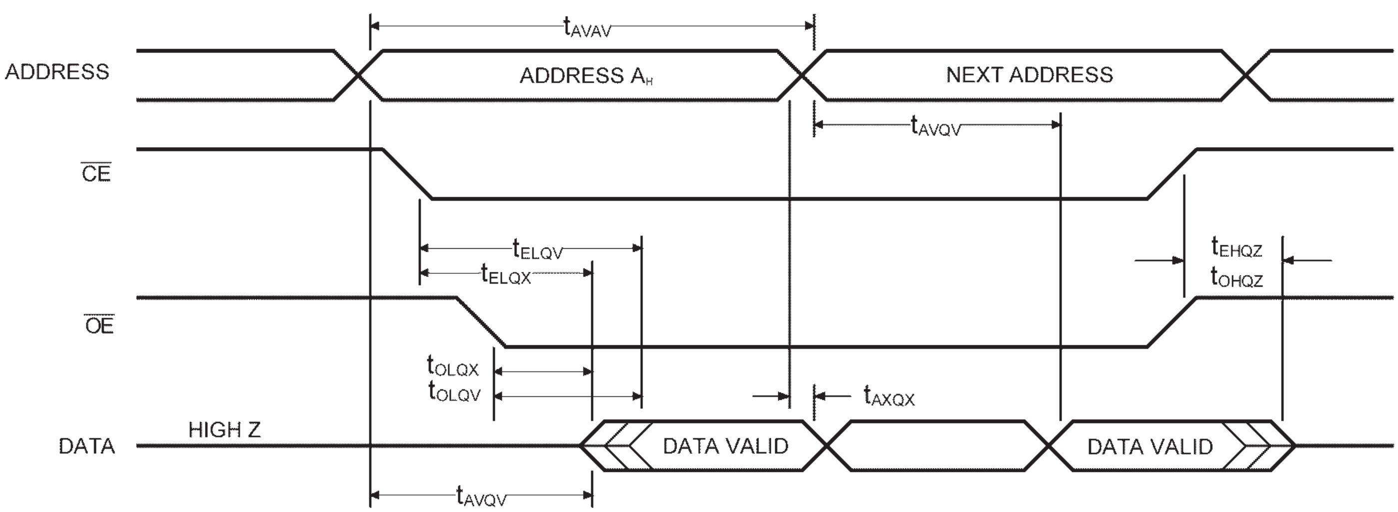
Symbol	Parameter	Max	Unit
t_{PUR}	Power-up to Read operation	100	µs
t_{PUW}	Power-up to Write operation	5	ms

AC ELECTRICAL CHARACTERISTICS—READ CYCLE

(V_{CC} = 5V ± 10%, All Temperature Ranges)[2]

Sym	Parameter	-150		-200		-250		-350		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{AVAV}	Read Cycle Time	150		200		250		350		ns
t_{AVQV}	Address Access Time		150		200		250		350	ns
t_{ELQV}	Chip Enable Access Time		150		200		250		350	ns
t_{OLQV}	Output Enable Access Time		70		80		100		100	ns
t_{ELQX}	Chip Enable to Output in Low Z	0		0		0		0		ns
t_{EHQZ}	Chip Disable to to Output in High Z		50		55		60		70	ns
t_{OLQX}	Output Enable to Output in Low Z	0		0		0		0		ns
t_{OHQZ}	Output Disable to Output in High Z		50		55		60		70	ns
t_{AVQX}	Output Hold from Address Change	0		0		0		0		ns

TIMING WAVEFORM OF READ CYCLE

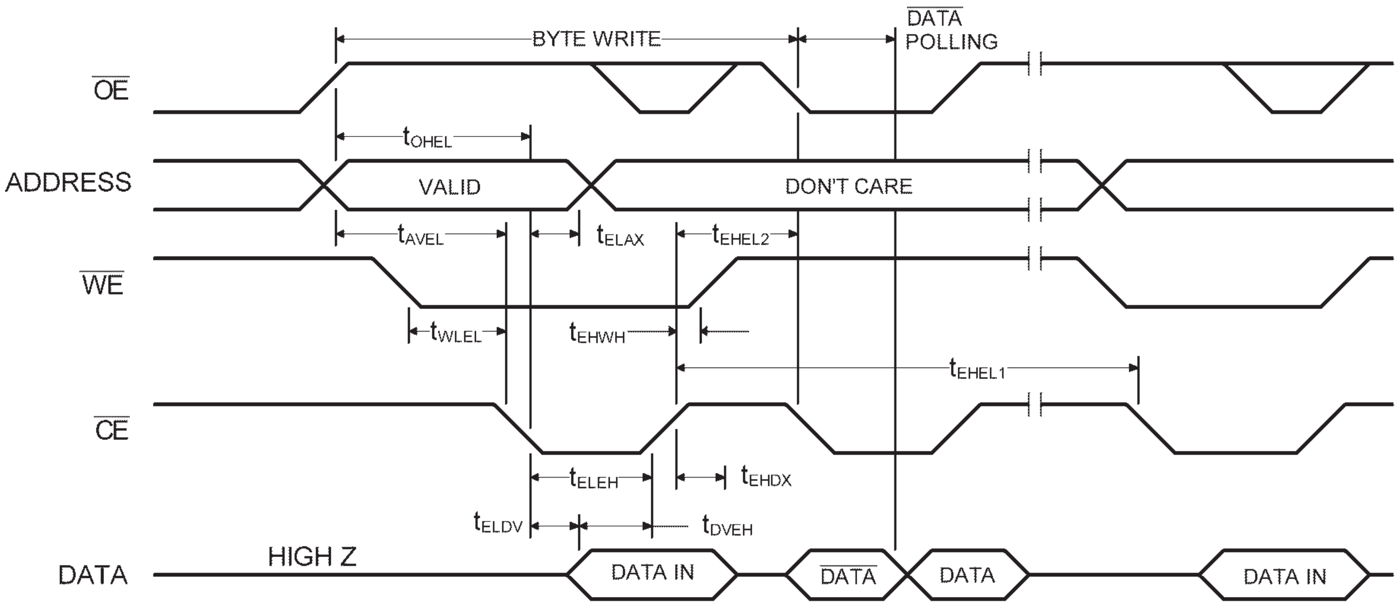


AC CHARACTERISTICS—WRITE CYCLE

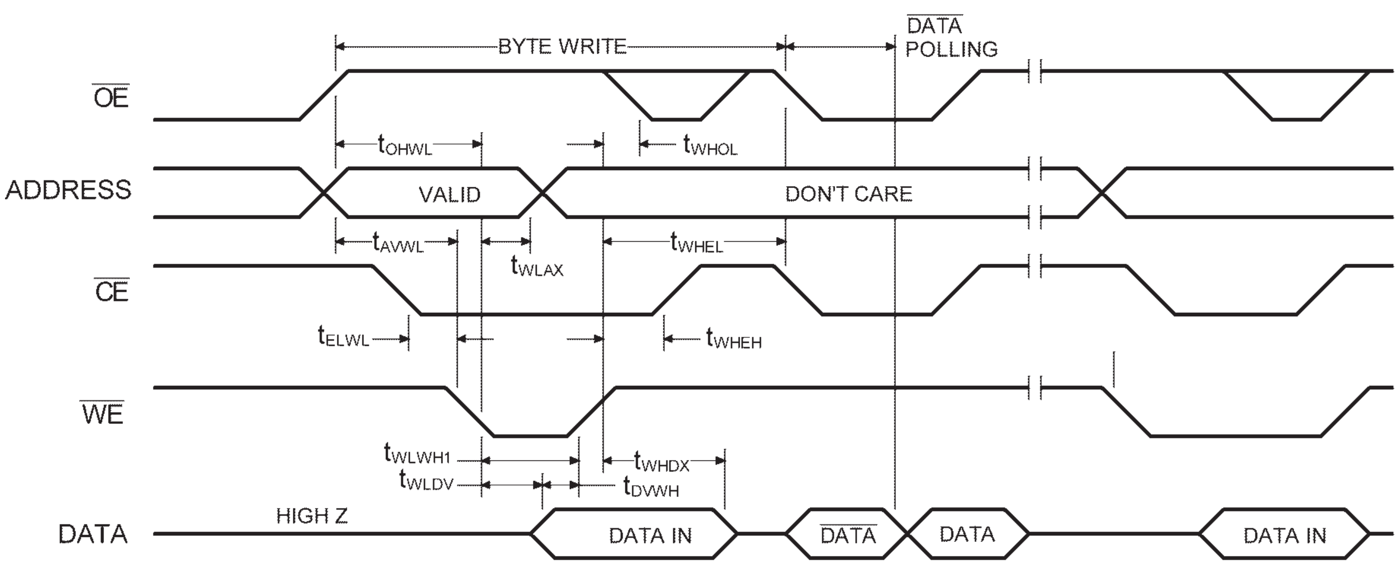
(V_{CC} = 5V ± 10%, All Temperature Ranges)(2)

Symbol	Parameter	150 / 200 / 250 / 350		Unit
		Min	Max	
t_{WHWL1} t_{EHEL1}	Write Cycle Time		10	ms
t_{AVEL} t_{AVWL}	Address Setup Time	0		ns
t_{ELAX} t_{WLAX}	Address Hold Time	50		ns
t_{WLEL} t_{ELWL}	Write Setup Time	0		ns
t_{WHEH}	Write Hold Time	0		ns
t_{OHEL} t_{OHWL}	$\overline{OE}$ Setup Time	10		ns
t_{WHOL}	$\overline{OE}$ Hold Time	10		ns
t_{ELEH} t_{WLWH}	$\overline{WE}$ Pulse Width	100		ns
t_{DVEH} t_{DVWH}	Data Setup Time	50		ns
t_{EHDX} t_{WHDX}	Data Hold Time	0		ns
t_{EHEL2} t_{WHWL2}	Byte Load Cycle Time	0.2	150	µs
t_{ELWL}	$\overline{CE}$ Setup Time	1		µs
t_{OVHWL}	Output Setup Time	1		µs
t_{EHWH}	$\overline{CE}$ Hold Time	1		µs
t_{WHOH}	$\overline{OE}$ Hold Time	1		µs

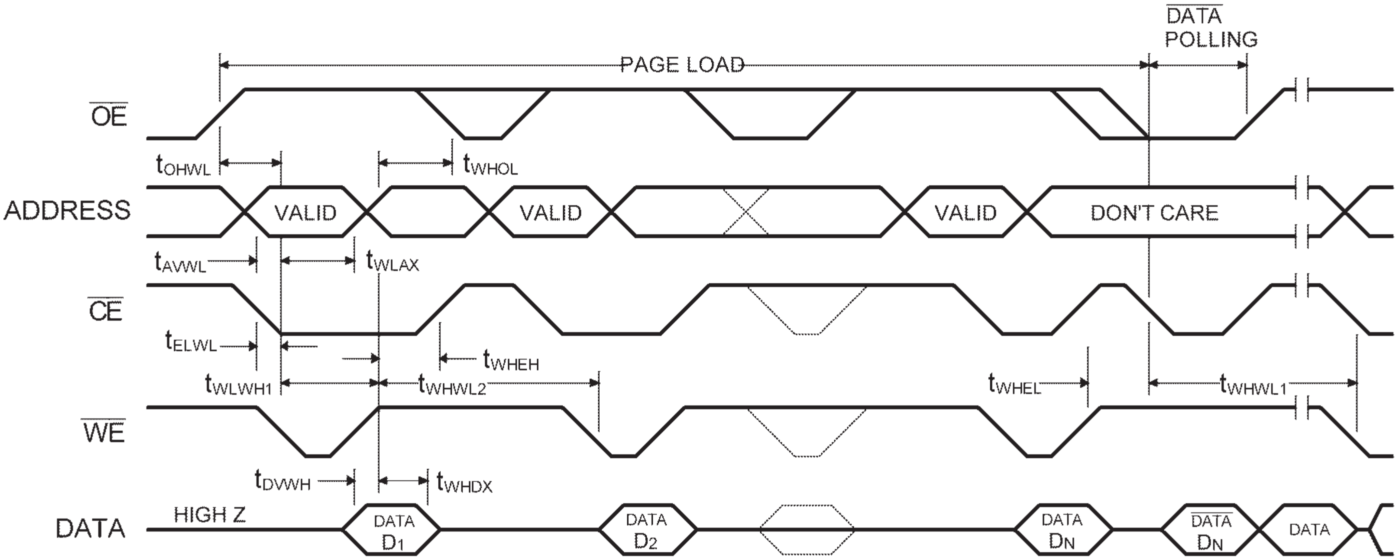
TIMING WAVEFORM OF BYTE WRITE CYCLE ($\overline{CE}$ CONTROLLED)



TIMING WAVEFORM OF BYTE WRITE CYCLE ($\overline{WE}$ CONTROLLED)



TIMING WAVEFORM OF PAGE WRITE CYCLE



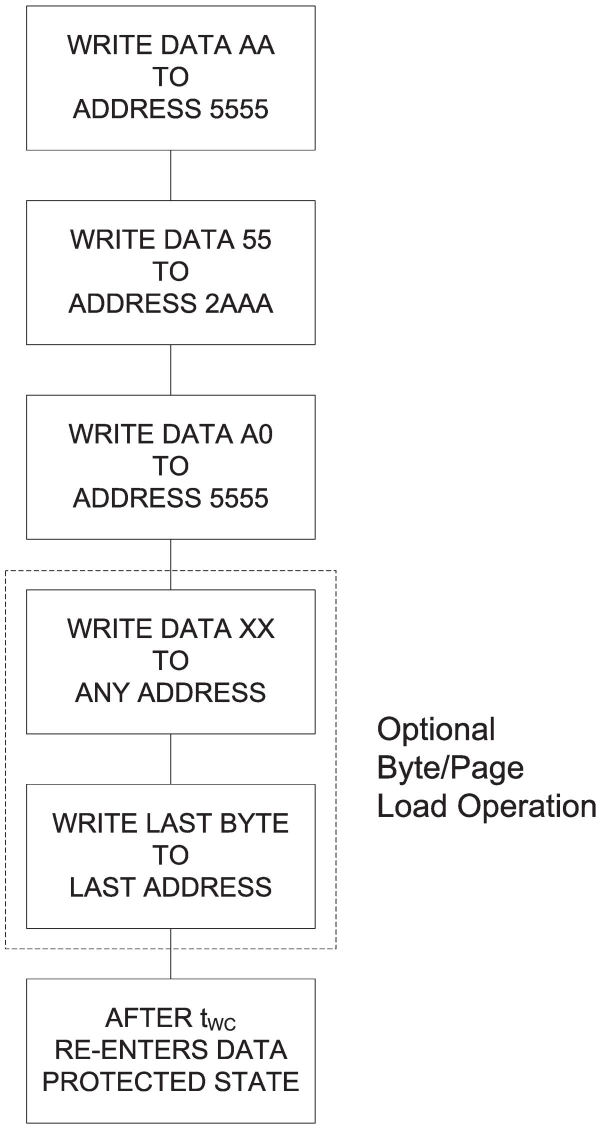
NOTES:

- For each successive write within the page write operation, A_6-A_{14} should be the same. Otherwise, writes to an unknown address could occur.

- Between successive byte writes within a page write operation, $\overline{OE}$ can be strobed LOW. For example, this can be done with $\overline{CE}$ and $\overline{WE}$ HIGH to fetch data from another memory device within the system for the next write. Alternatively, this can be done with $\overline{WE}$ HIGH and $\overline{CE}$ LOW, effectively performing a polling operation.

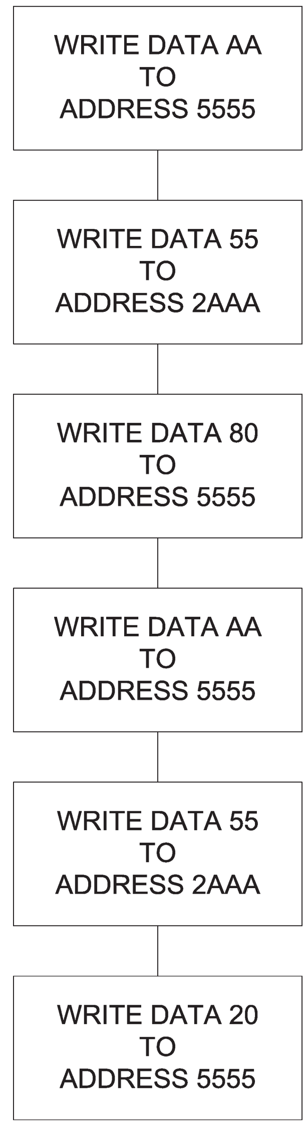
- The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to either the $\overline{CE}$ or $\overline{WE}$ controlled write cycle timing.

WRITE SEQUENCE FOR SOFTWARE DATA PROTECTION



(SDP Set)

SOFTWARE SEQUENCE TO DE-ACTIVATE SOFTWARE DATA PROTECTION



(SDP Reset)

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	10ns
Input Timing Reference Level	1.5V
Output Timing Reference Level	1.5V
Output Load	See Figure 1

TRUTH TABLE

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	**I/O**
Read	L	L	H	D_{OUT}
Write	L	H	L	D_{IN}
Write Inhibit	X	L	X	—
Write Inhibit	X	X	H	—
Standby	H	X	X	High Z
Output Disable	X	H	X	High Z

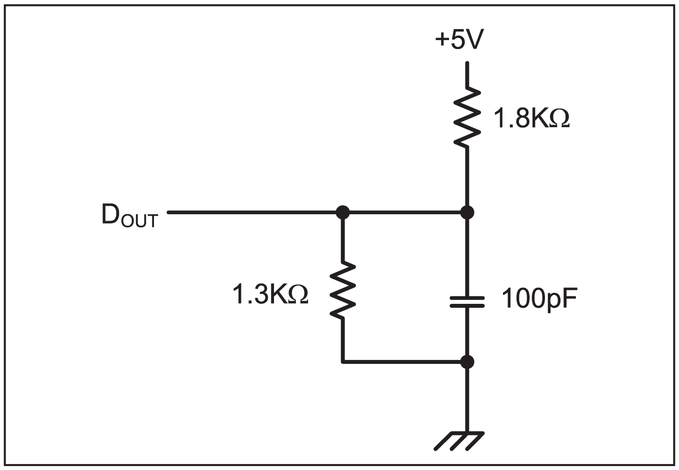


Figure 1. Output Load

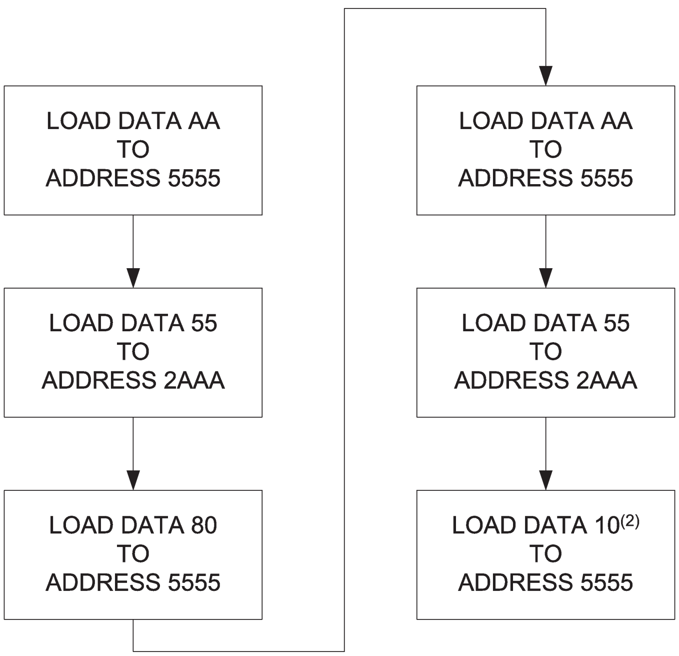
APPLICATION NOTE - SOFTWARE CHIP ERASE

The entire device can be erased at one time by using a 6-byte software code. The software chip erase code consists of 6-byte load commands to specific address locations with specific data patterns. Once the code has been entered, the device will set each byte to the high state (FFH). After the software chip erase has been initiated, the device will internally time the erase operation so that no external clocks are required. The maximum time required to erase the whole chip is t_{EC} (20 ms). The software data protection is still enabled even after the software chip erase is performed.

CHIP ERASE CYCLE CHARACTERISTICS

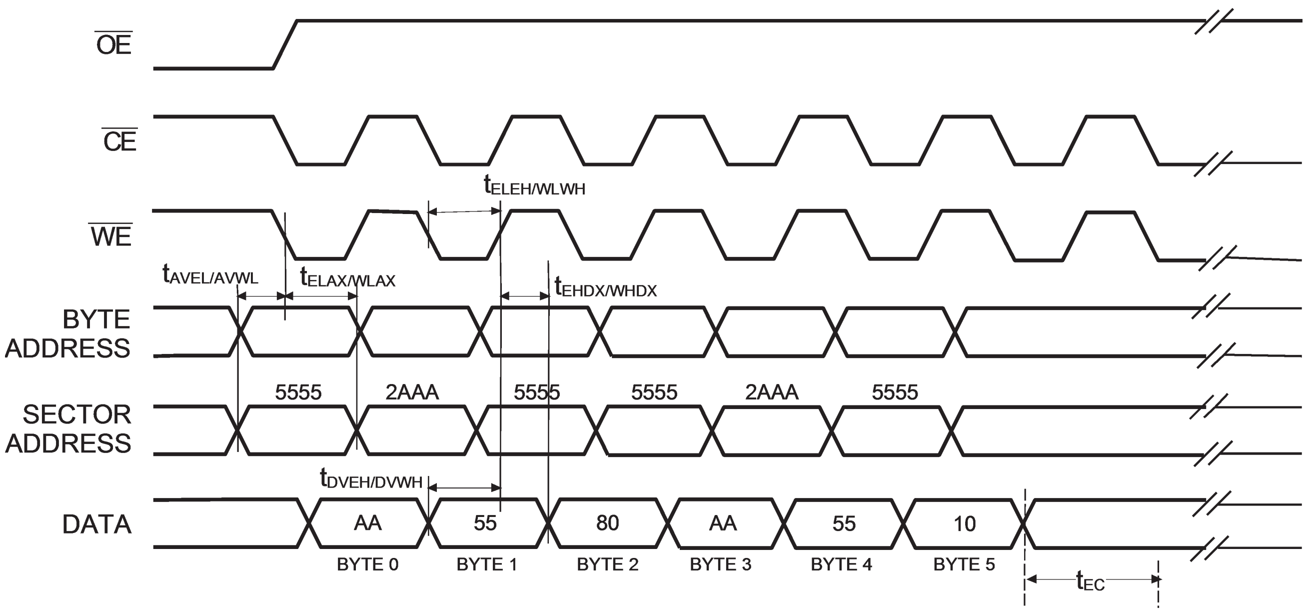
Symbol	Parameter	
t_{EC}	Chip Erase Cycle Time	20 ms Max

CHIP ERASE SOFTWARE ALGORITHM(1)(3)



Notes:
1. Data Format: (Hex); Address Format: (Hex).
2. After loading the 6-byte code, no byte loads are allowed until the completion of the erase cycle. The erase cycle will time itself to completion in 20 ms (max).
3. The flow diagram shown is for a x8 part. For a x16 part, the data should be 16 bits long (e.g., the data to be loaded should be AAAA for step 1 in the algorithm).

CHIP ERASE CYCLE WAVEFORMS



Notes:
1. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

ORDERING INFORMATION

PYA28C256	x	—	xx	x	x
Device Type	Endurance		Speed	Package	Processing

Processing

M	-55°C to +125°C
MB*	Test Method 5004 Process[1]

Package

CW	28-Pin Ceramic Side Brazed DIP, 600 mil
L	32-Pin Ceramic LCC, 450x550 mil

Speed

12, 15, 20, 25 (12 = 120 ns, etc.)

Endurance

Blank	10^4 Cycles
E	10^5 Cycles

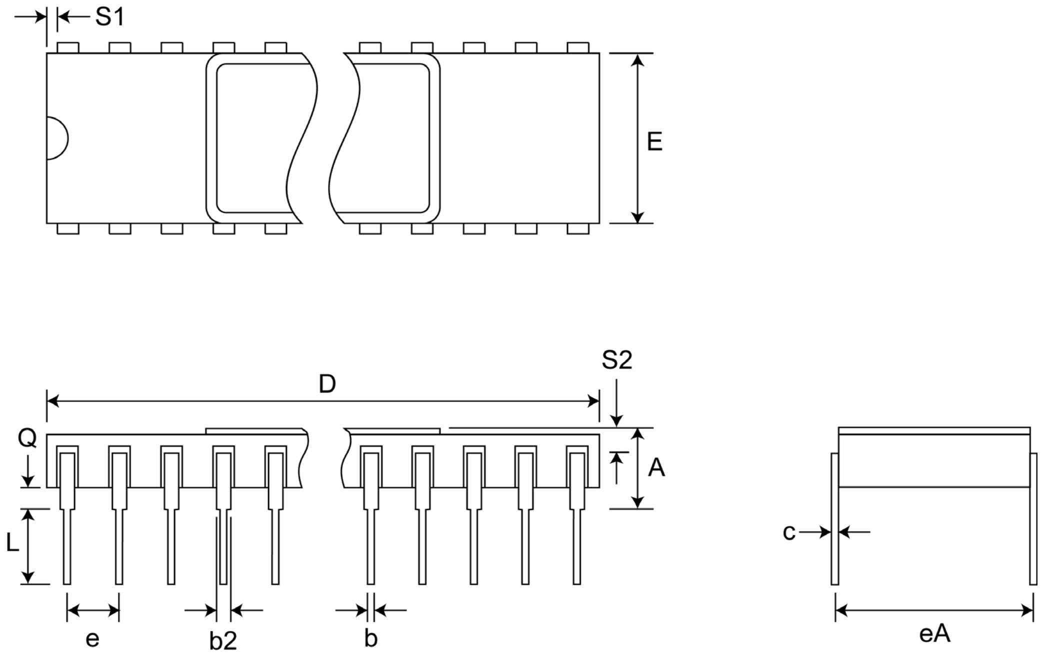
Device Type

32K x 8 EEPROM

[1] Parts are not MIL-STD-883 compliant. Parts are processed per Test Method 5004.

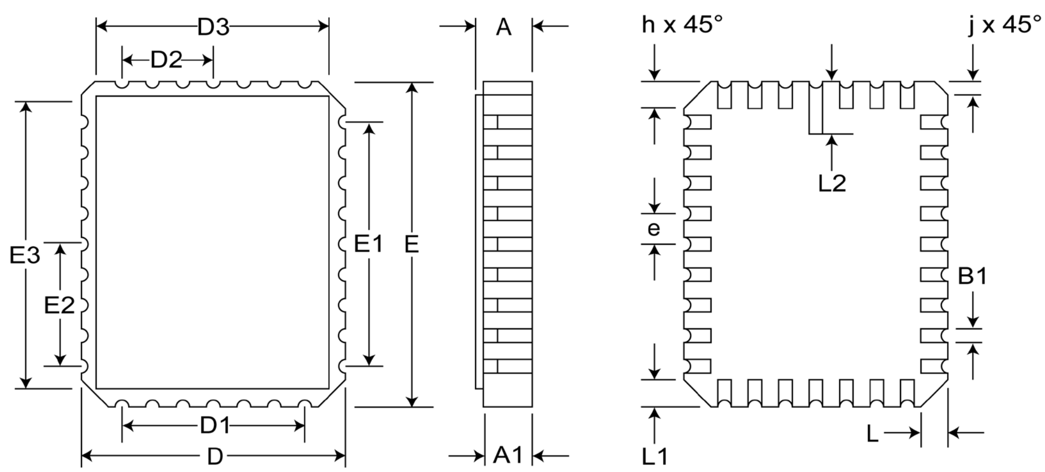
Pkg #	C5-1	
# Pins	28 (600 mil)	
Symbol	Min	Max
A	-	0.232
b	0.014	0.026
b2	0.045	0.065
C	0.008	0.018
D	-	1.490
E	0.500	0.610
eA	0.600 BSC	
e	0.100 BSC	
L	0.125	0.200
Q	0.015	0.060
S1	0.005	-
S2	0.005	-

SIDE BRAZED DUAL IN-LINE PACKAGE (600 mils)



Pkg #	L6	
# Pins	32	
Symbol	Min	Max
A	0.060	0.075
A1	0.050	0.065
B1	0.022	0.028
D	0.442	0.458
D1	0.300 BSC	
D2	0.150 BSC	
D3	-	0.458
E	0.540	0.560
E1	0.400 BSC	
E2	0.200 BSC	
E3	-	0.558
e	0.050 BSC	
h	0.040 REF	
j	0.020 REF	
L	0.045	0.055
L1	0.045	0.055
L2	0.075	0.095
ND	7	
NE	9	

RECTANGULAR LEADLESS CHIP CARRIER



REVISIONS

DOCUMENT NUMBER	EEPROM104
DOCUMENT TITLE	PYA28C256 - 32K x 8 EEPROM

REV	ISSUE DATE	ORIGINATOR	DESCRIPTION OF CHANGE
OR	Jan 2010	JDB	New Data Sheet
A	Mar 2012	JDB	Corrected typo in page header
02	Mar 2014	JDB	Replaced MIL-STD-883 Class B process flow with Test Method 5004
03	Jul 2014	JDB	
04	Jun 2023	JDB	Corrected typo in DC Electrical Characteristics table