Test Report

for

Single Event Effects Testing

of the

Performance Semiconductor (PACE) 1750AE Central Processing Unit

Prepared by

Scott Leavy
Honeywell Space Systems
July 31, 1998

1.0 Introduction

1.1 Purpose. The purpose of the test was to obtain SEU characterization data on the PACE 1750AE CPUs manufactured by Sarnoff for comparison to the original 1750A CPU manufactured by Westinghouse and the new 1750A CPU manufactured by Sarnoff.

1.2 1750AE CPU Test Results. The 1750AE CPU manufactured by Sarnoff is acceptable for use in the INU if the process parameters are consistent with the test samples. It is suggested (but not necessary) that the 1750AE device be further characterized at higher frequencies to help isolate the cause of the increased SEU susceptibility and to determine the frequency dependence of the SEU performance. This could become a larger issue if the MMU and PIC are transported to the same enhanced design/process.

1.3 Background. The Aerospace Corporation performed Single Event Effects (SEE) testing on the Performance Semiconductor 1750AE Central Processing Unit (CPU) for the Inertial Navigation Unit (INU) program. The 1750AE is a new (enhanced) design that was designed to improve the performance of the CPU. Ideally, the basic cell structures for the 1750AE device type should be the same as the original PACE CPU. In practice such a statement is not valid, hence testing was needed. The testing was performed by Rocky Koga and Susan Crain of Aerospace on 6/17/98 at the Berkeley 88" Cyclotron SEU Test Facility, which is located at University of California at Berkeley, CA.. Scott Leavy of Honeywell and Jim Elliot of Lockheed Martin witnessed the testing.

2.0 Test Article Descriptions

Two 1750AE CPUs were supplied by PACE for SEU testing. These reduced sample sizes were acceptable due to the high cost of each part and the high flip-flop count for each part. A large number of elements tested for each device, in effect, increases the statistical validity of the data. A total of 368 flip-flops were tested in each device. The 1750AE devices were reported to have the same process parameters as one of the 1750A CPUs that were also tested. Both of these were from the same wafer and were treated as one combined data set.

3.0 Test Procedures

The testing was performed using the same test configuration and test software that was used during the testing performed back in 1989 parts manufactured by Westinghouse. Since the purpose of this test was to compare the parts manufactured by Sarnoff to the parts manufactured by Westinghouse, duplicating all of the old test procedures and conditions was of prime importance. The parts were tested at room ambient temperature at 5V using Aerospace's BASACS tester. The software exercised the 23 mission critical 16 bit registers with alternating patterns of 5555hex and AAAAhex. In addition, the test exercised an unknown quantity of non-registered logic elements. These circuit elements could be susceptible to transient SEUs that could cause errors in the CPU. These effects were inherently included in the test results since there is no way to mask them out of the SEU data.

4.0 SEU Analysis

4.1 Analysis Method. The piece part test data summarized in paragraph 5.0 was analyzed to determine the predicted SEU rates for each device variety as compared to the old 1750A manufactured by Westinghouse. The summarized data set for each device variety was plotted and fitted to a Weibull distribution. The Weibull parameters were used along with the Space Radiation 4.0 program to calculate the predicted SEU rates for each device. The Space Radiation program was run using the Adam's 90% worst case environment at an inclination of 65 degrees. This orbit is specified in the INU specification. The Adam's 90% worst case terminology means that the cosmic ray environment will be less severe only 10% of the time. This does not account for potentially large fluxes of solar energetic particles that can result from large solar flare events. The total spacecraft and chassis shielding was assumed to be 100 mils of aluminum. This value should represent a nominal, but conservative value. It should be noted that galactic cosmic rays are not easily shielded. For instance, the SEU rates calculated for this report were decreased by less than 10% when the shielding value was increased to 200 mils of aluminum. If this analysis was performed for a device operation during a large solar flare event, shielding would become an issue because solar energetic particles are less penetrating (more easily shielded) than the galactic cosmic rays.

4.2 Weibull Distribution Defined. A Weibull distribution is a mathematical description of the failure behavior in a population of identical components. This distribution has been found to be a reasonable model for describing device failures due to single particles. The Weibull distribution defines the cross-section versus LET curve as a function of four parameters as follows:

$$\sigma(L)=\sigma_{sat}\,[1-\exp(-((L-L_0)/W)^S)]$$

Where
- σ_{sat} = Asymptotic Saturation Cross-section (cm^2)
- L_0 = Absolute LET Threshold ($MeV\text{-}cm^2/mg$)
- W = Statistical Width ($MeV\text{-}cm^2/mg$)
- s = Statistical Shape

4.3 Notes. It should be noted that the old 1750A SEU test data from 1989 was re-analyzed using the same guidelines so that an accurate SEU rate comparison could be made. The SEU rate calculation methods back in 1989 were not as accurate and tended to be more conservative. In addition, because the old analysis method used could not be understood based on the information available, the current analysis methods were the only way to get an accurate comparison between parts. The final analysis results will be incorporated into the next SEU Analysis update, which is scheduled for submittal later this year.

5.0 Test Results

5.1 Test Data Obtained. During the test the LET vs. cross-section data for the two parts were obtained along with the applicable test configuration and facility beam parameters. This test data is supplied in Appendix A.

5.2 Data Reduction. The SEU data was reduced and plotted to obtain the LET vs. cross-section curve for each data set. The data for the old 1750A is included to allow comparison of the characteristic curves. Each plot was then fitted to a separate Weibull curve. Figures 1 and 2 contain the Weibull curves for the old 1750A CPU and CPU #3 / CPU #4, respectively, along with the data for both test parts and the old 1750A CPU. All of the test data was shown on each curve to allows for an easier comparison from part to part. Table 1 summarizes the Weibull parameters obtained for each data set along with the Figure reference.

Table 1. Test Results Summary

Device	Saturation Cross-section (cm^2/device)	LET Threshold (MeV-cm^2/mg)	Weibull Width (MeV-cm^2/mg)	Weibull Shape	Figure Reference
Original CPU Data With BASACS	5.00E-6	35.0	37.0	2.0	1
CPU #3 PERF 03Z18AE 019 2 3	5.0E-6	15.0	30.0	1.5	4
CPU #4 PERF 03Z18AE 004 3 0	5.0E-6	15.0	30.0	1.5	4

5.3 Observations. From the LET vs. cross-section curves it was noticed that although the 1750AE devices were supposed to use the same cell structures and same process parameters as the CPU #2 1750A test sample (addressed in a separate test report), the LET thresholds were significantly lower and the saturation cross-sections were about 40% higher than CPU #2. The characteristic curves were also much steeper than those of the 1750A devices. In addition, the 1750AE devices appear to have two saturation areas. Between 30 and 40 MeV-cm^2/mg the curves appear to flatten, then rise again between 40 and 60 MeV-cm^2/mg. This characteristic could indicate that the 1750AE design has an increased susceptibility to transient SEUs. This explanation would also explain the decreased LET threshold. As can be seen, this conclusion that two saturation areas exist is not completely obvious and is not very conclusive. It is possible that this observation is not a true characteristic, but just an artifact of the test caused by ion/angle interactions. If this is the case, then the 1750AE flip-flops must just be more susceptible to bit flips than the 1750A flip-flops due to process parameters besides gate oxide thickness and L_{eff}. Testing is suggested to determine whether transient SEUs are an issue.

6.0 Analysis Results

6.1 Results Summary. Once the test data was reduced and the Weibull parameters were defined for each device type, the SEU rates were determined for the Adam's 90% worst case environment for a geosynchronous orbit at an inclination of 65 deg. These SEU results are shown in Table 2, along with all the parameters used to derive the SEU rates. The BASACS testing for the original PACE CPUs was also re-analyzed using the same analysis methods in order to obtain a good comparison of SEU rates. The relative differences between devices are given in the last column in Table 2. As can be seen, the calculated SEU rates for the 1750AE CPU test parts were significantly different than the parts originally tested during the testing in 1989. The two 1750AE CPUs demonstrated significantly increased SEU sensitivity. The calculated SEU rate for the 1750AE CPU was 16.5 times greater than the original 1750A CPU. However, if increased SEU transient susceptibility is the cause of the increased SEU susceptibility, the SEU rate could be highly frequency dependant. The original test hardware and software that were used in 1989 were used for this test to minimize cost and schedule. This configuration did not allow for testing at frequencies above 1.5MHz. Without test data it can be assumed (worst case) that the SEU transient rate scales directly with frequency. If this is the case the SEU could in effect be as high as 20 times higher for an application clock speed of 30MHz, resulting in a worst case rate of 3.47E-7 SEU/device-hr. Further testing would be needed to clarify SEU mechanisms and device SEU rate.

Table 2. Analysis Results Summary

Device	σ_{sat} (cm^2/ device)	L_o (MeV-cm^2/mg)	W (MeV-cm^2/mg)	s	Device Depth (μm)	Funnel Length (μm)	SEU Rate (SEU/ device-hr)	Factor vs. Original
Original CPU Data With BASACS	5.00E-6	35.0	37.0	2.0	0.5	0.0	1.13E-9	--
CPU #3 PERF 03Z18AE 019 2 3	5.0E-6	15.0	30.0	1.5	0.5	0.0	1.87E-8*	16.5*
CPU #4 PERF 03Z18AE 004 3 0	5.0E-6	15.0	30.0	1.5	0.5	0.0	1.87E-8*	16.5*

* See paragraph 6.1

6.2 Correlation to Design and Process Information. The data supplied by PACE does not clearly explain the increased SEU susceptibility of the 1750AE parts. The process information on the 1750AE devices indicates that they have the same gate oxide thickness and L_{eff} values as the 1750A CPU #2 test sample. The test/analysis results showed that the 1750AE has an SEU rate of almost three orders of magnitude greater than the CPU #2. The LET threshold was less, the cross-section was about 40% higher, and the characteristic curve was steeper in the SEU onset region. The LET spectrum in space has a significant drop-off in flux between 25 and 30 MeV-cm^2/mg. Because of this, the lower LET threshold and the steeper leading edge of the

response curve drive the large increase in SEU rate as opposed to the slightly increased cross-section.

The increased saturation cross-section and decreased LET threshold can be explained by two possible reasons. The first possible reason is that the new 1750AE design is susceptible to transient SEUs that have an LET threshold of less than the bit flip LET threshold of the flip-flop elements. This could also explain why there is a slight flat spot in the LET vs. cross-section curve between 30 and 40 MeV-cm^2/mg. In effect the transient SEU response curve and the bit flip SEU response curves would overlap. For this potential case, the device SEU rate would be highly dependant on clock speed. The second possible reason is that there are other undefined process differences between the CPU #2 part and the 1750AE parts that result in an increased bit flip SEU sensitivity. If this is the case, it is most likely the result of a change in process targeted at increasing the speed of the flip-flop elements. For a given technology, increased speed typically leads to increased SEU susceptibility. Increased speed usually is the result of decreased capacitance (decreased critical charge) or decreased delay time (decreased response time) of the individual gates. For this potential case, the device SEU rate would then be lightly dependant or not dependant on clock speed. It should be noted that 48 more registers are used in the 1750AE design as compared to the 1750A design. This factor could cause a slight increase in saturation cross-section, but could not be the cause of the decreased LET threshold.

7.0 Conclusions and Recommendations

Based on the test and analysis results, the 1750AE CPU device fabricated by Sarnoff is acceptable for use in the INU FCSP and IMSP assemblies. The 1750AE displayed an SEU rate of about 16.5 times greater than the original 1750A manufactured by Westinghouse. If increased SEU transient susceptibility is the cause, the SEU rate could be as high as 3.47E-7 SEU/device-hr. This value is 0.87% of the SEU rate specification limit of 4E-5 SEU/hr. This would be acceptable based on the current design. It might be advisable to test the 1750AE under various frequencies to determine the actual expected SEU rate at frequency. This is especially true if the MMU and PIC are planned for upgrade to the enhanced design. The INU would not be able to tolerate increased SEU rates for all three devices in the processor chip-set.

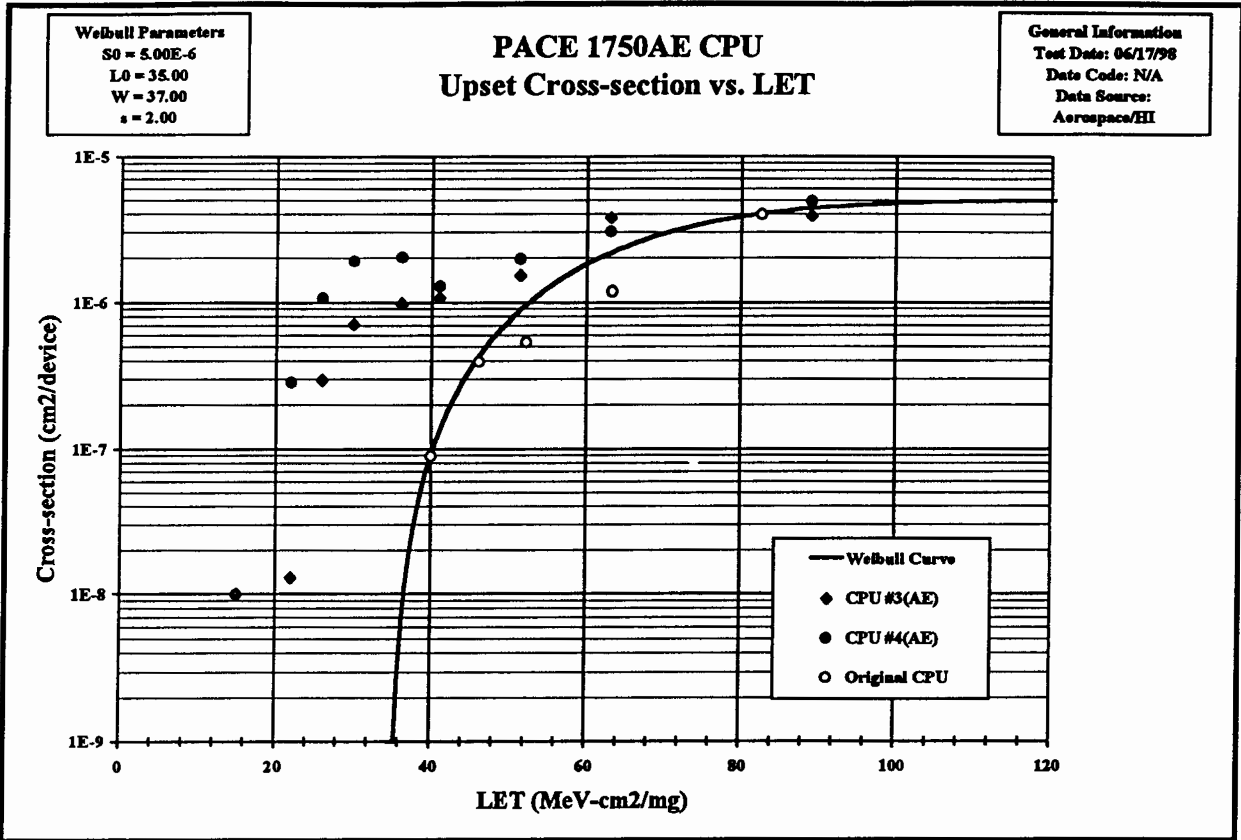

Figure 1. Weibull Curve Fit for the Original CPU

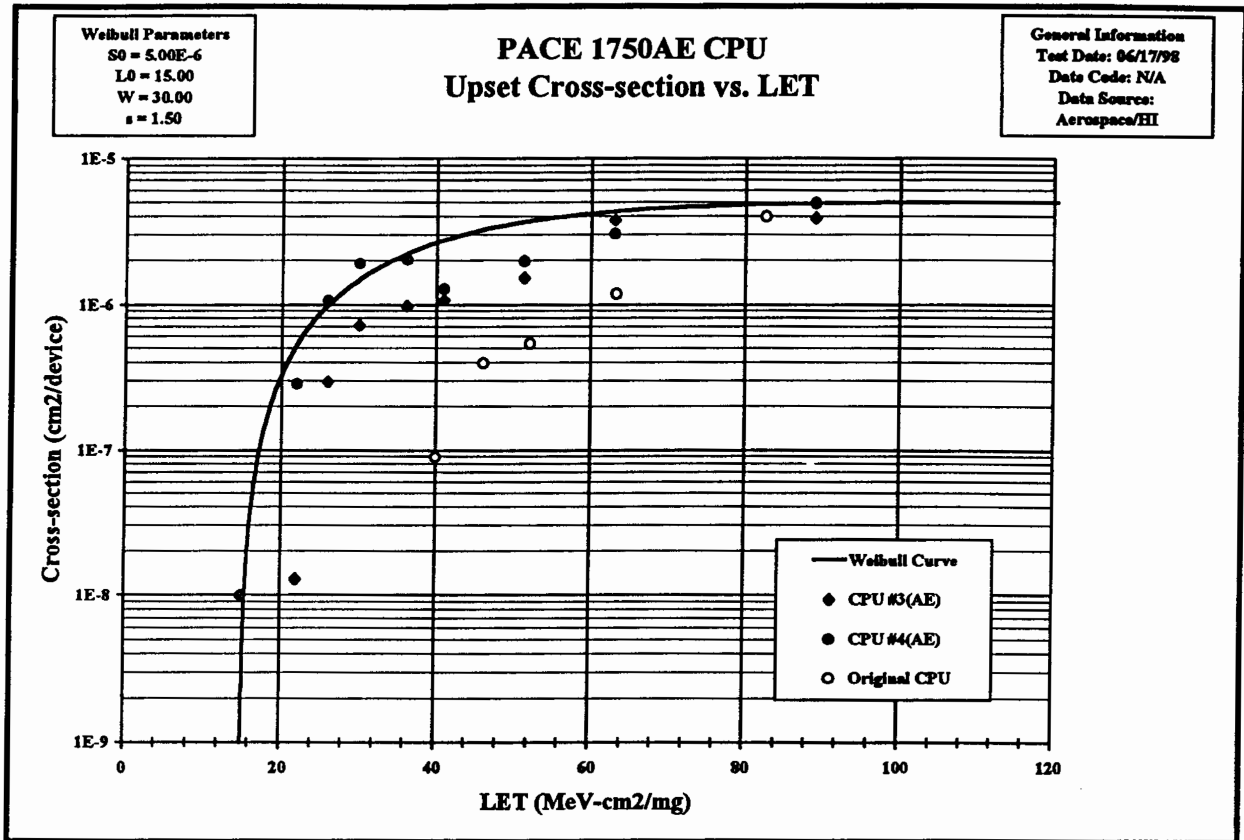

Figure 2. Weibull Curve Fit for CPU #3 and 4