APPLICATION NOTE
PACE P1754 PIC
SYSTEM TEST

The PACE1754 PIC chip provides the system designer with a system test which may be run at power-up if enabled. This test is very useful for establishing the functionality of the P1750A/AE CPUs, P1753 COMBO, and the P1754 PIC as well as their interconnection. When enabled and successfully completed, the test provides a good indication that basic system operation is possible.

Section 1 – System Test Description

The PIC system test is designed to be a go/no-go test run only at power-up. It is neither a diagnostic tool nor a periodic built-in test and should not be used as such. It is a very powerful feature when used as intended.

1.1 Test Operation

The P1754 PIC contains a 4k x 16 bit ROM which stores the PIC test in the form of a 1750A assembly language program. The PIC also contains a small RAM which covers several non-sequential addresses to provide a place for the CPU to read and write data. This program and RAM, in conjunction with several hardware provisions in the PIC and COMBO, make up the system test.

The system test is designed to operate automatically after completion of the P1750A CPU power-up built-in-test and initialization. After reset is released, the P1750A CPU automatically runs a built-in-test prior to the assertion of the NML PWRUP (normal power-up) signal. Following this signal, the CPU begins execution of the MIL-STD-1750A initialization sequence to make the state of the machine match the reset state specified by the standard. At the end of this sequence, the P150A begins normal operation from address 0, fetching and executing the instruction stored there.

If the PIC system test is enabled ($\overline{\text{TEST ON}}$), it will begin executing at this point. The PIC will feed the IB bus with the instruction and operand data in place of the system memory, which is disabled during the test. If $\overline{\text{TEST ON}}$ is HIGH, the test will not be executed and the CPU will begin running the system code out of the system memory. The test extensively exercises the P1750A/AE CPUs, P1754 PIC, and P1753 COMBO as well as the IB bus and strobes. During this time, the TEST END signal will be LOW.

When the test has completed, the result will be provided as an output to the PIC Status Register (9F41) and TEST END will be asserted. The most significant three bits of the Status Register correspond to the test results of the CPU, COMBO and PIC respectively with a logic 1 indicating a passing condition. After assertion of TEST END the CPU will again begin instruction fetch and execution from memory location 0, but this time the system memory will be enabled allowing the system to begin the user program.

1.2 Test Sequence

The program flow of the PIC system test is illustrated in Figure 1.1. The test begins by initializing the system to provide 1 data wait state and 0 address wait states, sets up the correct interrupt mask, and halts both Timer A and Timer B. The test then verifies proper operation of the CPU, exercising it more extensively than the CPU self test that is built in to the P1750A/AE. First, operation of the data transfer and jump instructions is verified, followed by the operation of the arithmetic functions, interrupts and BEX instruction. After conclusion of the CPU tests, the result (pass or fail) is output to the PIC Status Register using an I/O output command to address 1F41 with bit 0=0 for fail or bit 0=1 for pass.

Once the proper operation of the CPU has been verified, the program begins to test the PIC itself. A checksum of the ROM containing the test is performed and the results verified to assure that the program is correctly stored. The registers are then tested by writing and verifying several patterns in each of them. Once the registers are verified, the

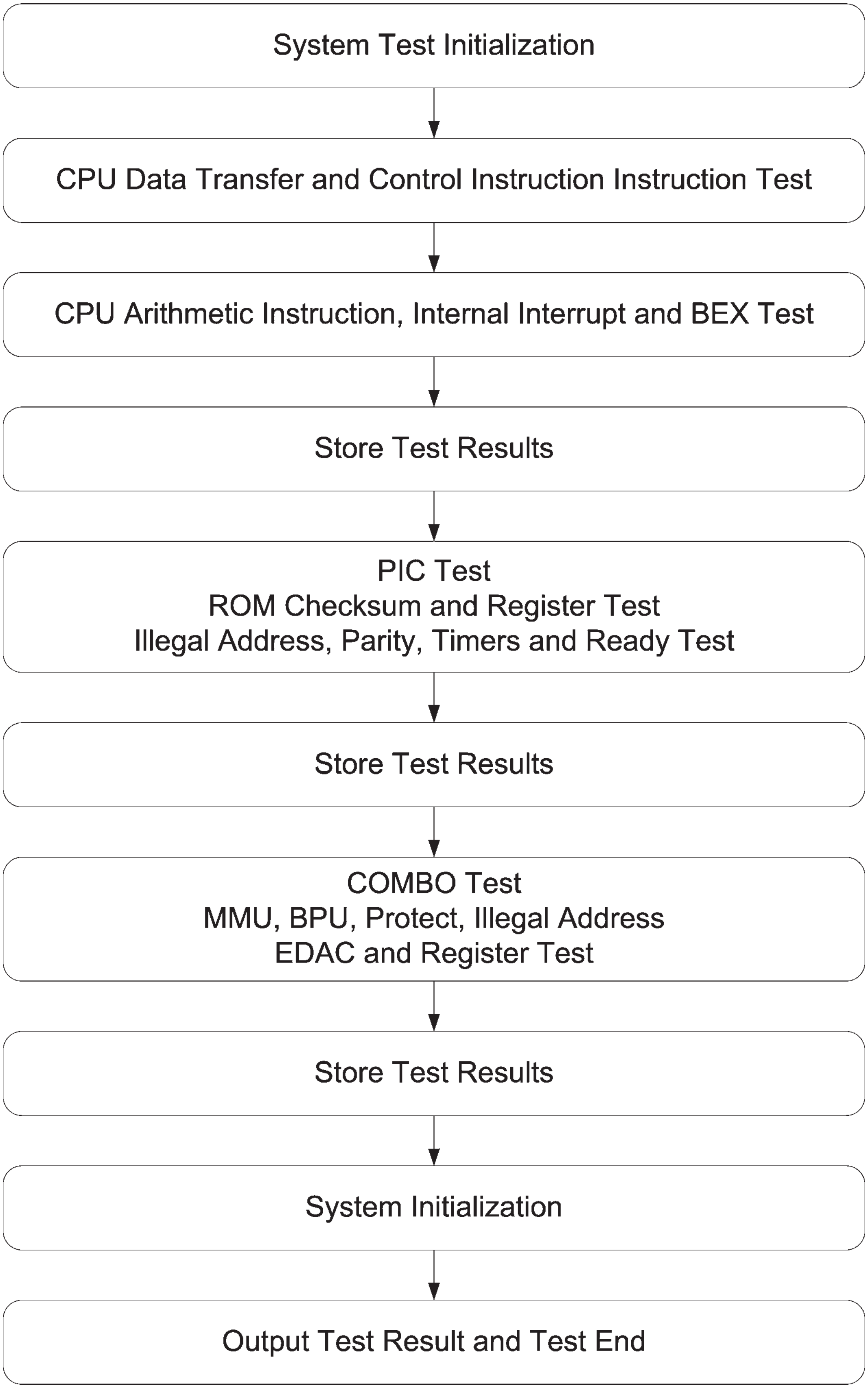
System Test Initialization
CPU Data Transfer and Control Instruction Instruction Test
CPU Arithmetic Instruction, Internal Interrupt and BEX Test
Store Test Results
PIC Test
ROM Checksum and Register Test
Illegal Address, Parity, Timers and Ready Test
Store Test Results
COMBO Test
MMU, BPU, Protect, Illegal Address
EDAC and Register Test
Store Test Results
System Initialization
Output Test Result and Test End

Figure 1.1 System Test Flow

illegal address detection circuitry is tested by programming 2 unimplemented memory holes as described in the PIC data sheet and reading from addresses within the holes. This is verified to cause an External Address Error. The parity generation and checking logic on the PIC is then tested utilizing the small RAM memory located on the PIC chip. Data patterns are loaded into the RAM and the parity signal inverted to force a parity error, which is verified to occur. The Bus Timer and System Watchdog Timer are then checked by forcing each to time out and verifying that the proper bit is set in the PIC status register. Finally, the Ready generation logic is tested and verified. After conclusion of the PIC test, the PIC Status Register is updated to include the PIC result using another output to address 1F41 with bit 2=1 for pass or 0 for fail along with the CPU result stored earlier in bit 0.

The program now tests the COMBO, the third element of the PACE 1750A system. First, the MMU memory is tested by writing a pattern into each location of the RAM and reading it back to verify the pattern stored equals the pattern received. The MMU protection feature is then tested by performing a memory write through the MMU with an Access and Key Code mismatch. The write is verified to have been prevented. Next, the BPU memory is tested by writing and verifying a data pattern in each location, similar to the MMU memory test. Then the functionality of the BPU is tested for CPU memory write protection by setting and resetting the protection for each 1k memory page in the first 64k of memory and verifying that a write to that page is properly allowed or prevented. Note that the DMA portion of the BPU is not tested since there is no DMA channel within the CPU, PIC or COMBO to exercise it with. The External Address Error detection logic is then tested for both memory and I/O reads and writes. The I/O is tested by performing accesses to the addresses defined by MIL-STD-1750A as reserved and by setting the Last Implemented I/O address registers (1F57 and 1F58) as described in the COMBO data sheet to specify a legal range and then accessing outside that range. Both of these actions are verified to cause an error. The memory is tested by specifying unimplemented memory blocks in the Unimplemented Memory registers (1F55 and 1F56) as described in the COMBO data sheet and performing accesses to those blocks. This is also verified to cause the error. Next, the MMU cache logic is tested by accessing a memory address located on the 4k page currently addressed by the page register in the cache (cache hit) and verifying the correct extended address, and then accessing a memory address not on the 4k page currently addressed by the page register in the cache (cache miss) and verifying the correct extended address. Finally, the EDAC function is tested by forcing a single bit error in RAM, once on each of the 16 data bits, and verifying that the COMBO makes the proper correction. After the conclusion of this test, the PIC Status Register (1F41) is again updated with the test results by setting bit 1=1 for a pass and bit 1=0 for a fail.

The PIC test now concludes by initializing the 1750A system back to the reset state specified by the 1750A standard. The PIC timer clock frequency is set to 0, disabling the timer clock output. The COMBO is programmed to provide three address wait states, and the PIC is programmed to provide 15 data wait states on all four quarters of memory to accommodate the slowest of system memories until the actual required number of wait states can be programmed by the system software. Both the COMBO and PIC are programmed to disable both parity and EDAC and the PIC Control Register is set to all 0’s. Finally, a jump to address 0 is placed in the instruction pipeline and TEST END is issued, after which all instruction fetches will take place from the user memory rather than the PIC ROM.

The duration of the test including the CPU self test is 216,652 clocks without the MMU and 508,040 clocks with the MMU. This translates to the times listed in the table below.

CLK	With MMU	Without MMU
20 Mhz	25.4 ms	10.8 ms
30 Mhz	16.9 ms	7.2 ms
40 Mhz	12.7 ms	5.4 ms

Section 2 – Design Considerations

To insure successful operation of the PIC system test, special care must be taken to properly connect the PIC, COMBO, and CPU together. The most common cause of system test failures in first-run designs is the improper connection of the various bus and control signals among the three chips.

2.1 Test On

The test enable signal ($\overline{\text{TEST ON}}$) must be LOW to execute the test. It is not necessary to pull it back up after test completion, however. The test will complete and normal operation will begin even if the signal is simply grounded.

2.2 Reset and CPU Clock

The $\overline{\text{RESET}}$ signal and CPU clock must be connected to the CPU, PIC and COMBO inputs such that the signals are the same on each component. The $\overline{\text{RESET}}$ must be an active-LOW pulse of at least 25ns, 17ns or 13ns at 20Mhz, 30Mhz and 40Mhz respectively.

2.3 Bus Control Lines

It is important that the five bus control lines (STRBA, $\overline{\text{STRBD}}$, R/$\overline{\text{W}}$, D/$\overline{\text{I}}$ and M/$\overline{\text{IO}}$) be directly connected among the chips during the test. Any external gating or drivers on these signals must be inactive during the test.

2.4 Ready Generation

The RDYD signal must be sourced by the PIC and the RDYA signal must be sourced by the COMBO during the test. Any external logic generating these signals must be disabled until completion of the test. The external ready (EX RDY) input to the PIC must be sourced by the COMBO and the external ready 1 ($\overline{\text{EX RDY}}_1$) signal must be LOW during the test.

2.5 EDAC Signals

The Error Detection and Correction (EDAC) handshake signals (SING ERR and RAM DIS) must be connected between the PIC and COMBO even if the EDAC function is not used by the system. The test will indicate a COMBO failure if these signals are not connected since the EDAC logic is exercised during the test.

2.6 Bus Arbitration Signals

The bus must be granted to the CPU during the test ($\overline{\text{BUS GNT}}$ must be LOW and $\overline{\text{BUS LOCK}}$ must be pulled up). If the bus arbiter in the COMBO is used, the correct $\overline{\text{BUS REQ}}$/$\overline{\text{BUS GNT}}$ pair must be connected between the CPU and COMBO and no higher priority requests should be allowed. If the arbiter in the COMBO is not used, the CPU must be assured of having access to the bus during the test by other means.

2.7 DMA Acknowledge

The DMA ACK input to the COMBO must indicate that DMA is not active during the test.

2.8 Console Mode

The CON REQ input to the CPU must remain inactive until after test completion.

2.9 Interrupts and Faults

The User, I/O and Power Down interrupt inputs to the CPU must remain inactive during the test. The five fault inputs (MEM PRT ER, MEM PAR ER, EXT ADR ER, SYS FLT_0 and SYS FLT_1) must also remain inactive during the test. TEST END may be used to guarantee the inactive state.

2.10 Information and Status Buses

The Information Bus (IB_0-IB_{15}) and Status Bus (AS_0-AS_3 and AK_0-AK_3) signals must be connected among the PIC, COMBO and CPU directly and all other drivers must be disabled during the test. The access key (AK_0-AK_3) must be connected even if the MMU is not used by the system since the MMU is exercised during the test.

2.11 Test End

The TEST END signal from the PIC is the indication that the system test is complete. It can be used to assure that any logic capable of driving the above signals or changing their timing is held inactive until after test completion. It should also be used to disable the system memory.

2.12 Fault Indication

At the end of the test, the test results are written to the PIC status register (1F41) and may be read by the user program by an XIO RA, :9F41 command. If it is desired to have a hard fault indicator, a pulse to the INTA signal is provided during the time that the test results appear on the IB bus such that they may be latched into a register on the rising edge of that signal. If this is implemented, the INTA signal should be qualified by the TEST END signal to avoid latching the IB bus into the register each time the INTA signal is valid (during the interrupt response cycle in normal operation).

Section 3 – Fault Coverage

The PIC system test was carefully designed with the hardware features of the PIC, COMBO and CPU in mind to obtain the highest possible fault coverage within the constraints of ROM size and signal access. The resulting test is quite comprehensive.

Though not every 1750A instruction is executed, the instructions chosen for the test exercise most of the microcode paths through the CPU which, in conjunction with the CPU built-in-test, exercises most of the circuitry within the chip. The hardware that is not tested includes the console mode logic, since it is not known if a console interface has been implemented by the system, and the timers (A and B) since it is not known yet what clock frequency is being used.

The PIC itself is quite thoroughly tested. Most major logic blocks (the ROM, registers, illegal address detection, parity, timers and ready generation) are tested. The hardware that is not tested includes the timer clock output, for the same reason that the A and B timers are not tested, the illegal I/O detection logic, the First Failing Memory Address register and the tri-state control logic since it is impossible to determine if a signal has become high-impedance from inside the chip.

The COMBO is also well tested with good tests of the MMU and BPU memories and protection, the illegal address detection logic, the error detection and correction logic, and the registers. The areas of the COMBO which are not tested include the parity logic, the block protection logic for DMA writes and the various DMA operation modes since there is no DMA channel available for the test, the bus arbiter, since it is not known whether the arbiter is being used by the system, and the operation of the Memory Fault Status Register (MFSR) and EDAC fault address and data registers.

REVISIONS

DOCUMENT NUMBER:	ANP16-001
DOCUMENT TITLE:	APPLICATION NOTE - P1754 SYSTEM TEST

REV.	ISSUE DATE	ORIG. OF CHANGE	DESCRIPTION OF CHANGE
ORIG	May-89	RKK	New Data Sheet
A	Oct-05	JDB	Added Pyramid logo