

### FEATURES

- Fast Access Times - 10/12/15/20 ns
- Low Power Operation
- Single 3.3V ± 0.3V Power Supply
- 2.0V Data Retention
- Easy Memory Expansion Using  $\overline{CE}$  and  $\overline{OE}$  Inputs
- Fully TTL Compatible Inputs and Outputs
- Advanced CMOS Technology
- Fast  $t_{OE}$
- Automatic Power Down when deselected
- Packages
  - 44-Pin TSOP II



### DESCRIPTION

The P3C1041 is a 262,144 words by 16 bits high-speed CMOS static RAM. The CMOS memory requires no clocks or refreshing, and has equal access and cycle times. Inputs are fully TTL-compatible. The RAM operates from a single 3.3V ± 0.3V tolerance power supply.

Access times as fast as 10 nanoseconds permit greatly enhanced system operating speeds. CMOS is utilized to reduce power consumption to a low level.

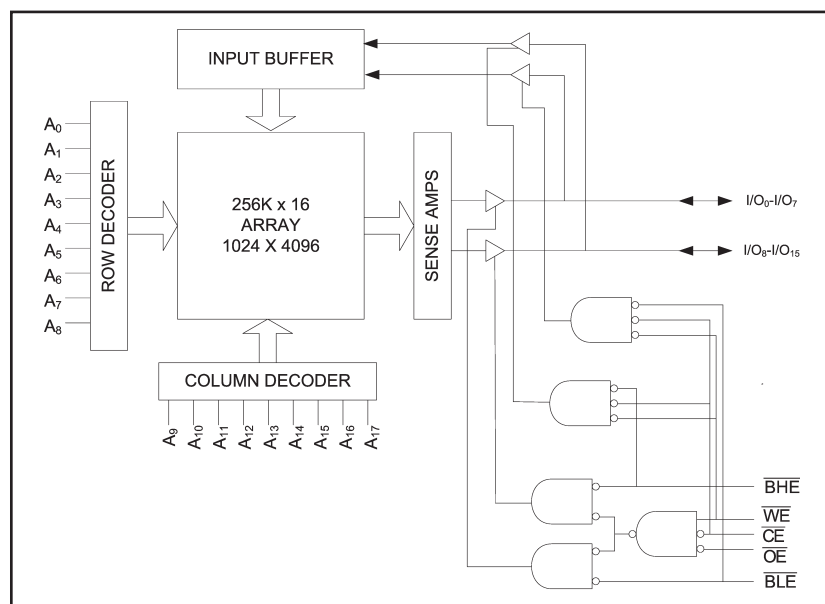
The P3C1041 device provides asynchronous operation

with matching access and cycle times. Memory locations are specified on address pins  $A_0$  to  $A_{17}$ . Reading is accomplished by device selection ( $\overline{CE}$ ) and output enabling ( $\overline{OE}$ ) while write enable ( $\overline{WE}$ ) remains HIGH. By presenting the address under these conditions, the data in the addressed memory location is presented on the data input/output pins. The input/output pins stay in the HIGH Z state when either  $\overline{CE}$  or  $\overline{OE}$  is HIGH or  $\overline{WE}$  is LOW.

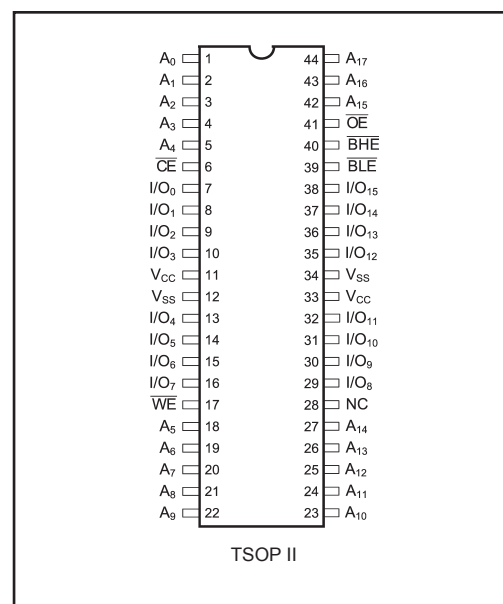
The P3C1041 is packaged in a 44-pin 400-mil wide TSOP II package.



### FUNCTIONAL BLOCK DIAGRAM



### PIN CONFIGURATION





## MAXIMUM RATINGS<sup>(1)</sup>

Sym	Parameter	Value	Unit
$V_{CC}$	Power Supply Pin with Respect to GND	-0.5 to +4.6	V
$V_{TERM}$	Terminal Voltage with Respect to GND (up to 7.0V)	-0.5 to $V_{CC} + 0.5$	V
$T_A$	Operating Temperature	-55 to +125	°C
$T_{BIAS}$	Temperature Under Bias	-55 to +125	°C
$T_{STG}$	Storage Temperature	-65 to +150	°C
$I_{OUT}$	DC Output Current	20	mA

## RECOMMENDED OPERATING CONDITIONS

Grade <sup>(2)</sup>	Ambient Temp	GND	$V_{CC}$
Commercial	0°C to 70°C	0V	3.3V ± 10%
Industrial	-40°C to +85°C	0V	3.3V ± 10%

## CAPACITANCES<sup>(4)</sup>

( $V_{CC} = 3.3V$ ,  $T_A = 25^\circ C$ ,  $f = 1.0MHz$ )

Sym	Parameter	Conditions	Typ	Unit
$C_{IN}$	Input Capacitance	$V_{IN} = 0V$	8	pF
$C_{OUT}$	Output Capacitance	$V_{OUT} = 0V$	8	pF

## DC ELECTRICAL CHARACTERISTICS

(Over Recommended Operating Temperature & Supply Voltage)<sup>(2)</sup>

Sym	Parameter	Test Conditions	Min	Max	Unit
$V_{IH}$	Input High Voltage		2.0	$V_{CC} + 0.3$	V
$V_{IL}$	Input Low Voltage		-0.3 <sup>(3)</sup>	0.8	V
$V_{OL}$	Output Low Voltage (TTL Load)	$I_{OL} = +8\text{ mA}$ , $V_{CC} = \text{Min}$		0.4	V
$V_{OH}$	Output High Voltage (TTL Load)	$I_{OH} = -4\text{ mA}$ , $V_{CC} = \text{Min}$	2.4		V
$I_{LI}$	Input Leakage Current	$V_{CC} = \text{Max}$ . $V_{IN} = \text{GND to } V_{CC}$	-1	+1	μA
$I_{LO}$	Output Leakage Current	$V_{CC} = \text{Max}$ . $\overline{CE} = V_{IH}$ , $V_{OUT} = \text{GND to } V_{CC}$	-1	+1	μA
$I_{SB}$	Standby Power Supply Current (TTL Input Levels)	$\overline{CE} \geq V_{IH}$ $V_{CC} = \text{Max}$ . $f = \text{Max.}$ , Outputs Open $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$	—	20	mA
$I_{SB1}$	Standby Power Supply Current (CMOS Input Levels)	$\overline{CE} \geq V_{CC} - 0.2V$ $V_{CC} = \text{Max}$ . $f = 0$ , Outputs Open $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$	—	10	mA

**POWER DISSIPATION CHARACTERISTICS VS. SPEED**

Sym	Parameter	Temperature Range	-10	-12	-15	-20	Unit
I <sub>CC</sub>	Dynamic Operating Current*	Commercial	90	80	70	60	mA
		Industrial	N/A	95	85	75	mA

\* V<sub>CC</sub> = 3.6V. Tested with outputs open. f = Max. Switching inputs are 0V and 3V.  $\overline{CE} = V_{IL}$ ,  $\overline{OE} = V_{IH}$ .

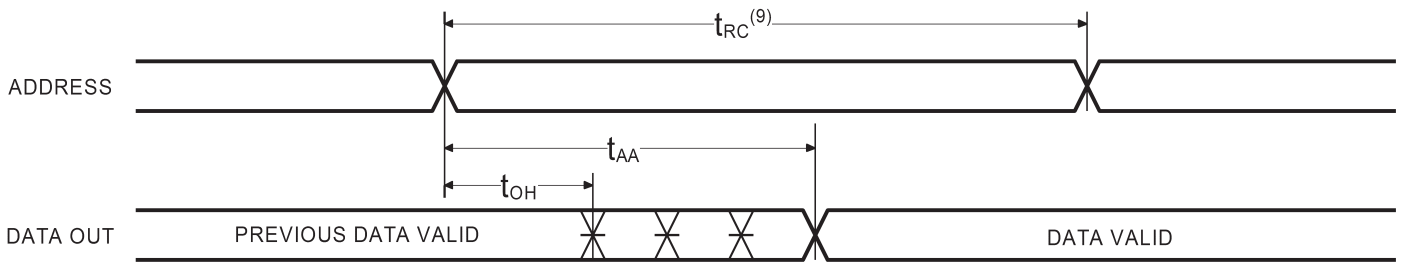
**AC ELECTRICAL CHARACTERISTICS—READ CYCLE**

(V<sub>CC</sub> = 3.3V ± 0.3V, All Temperature Ranges)<sup>(2)</sup>

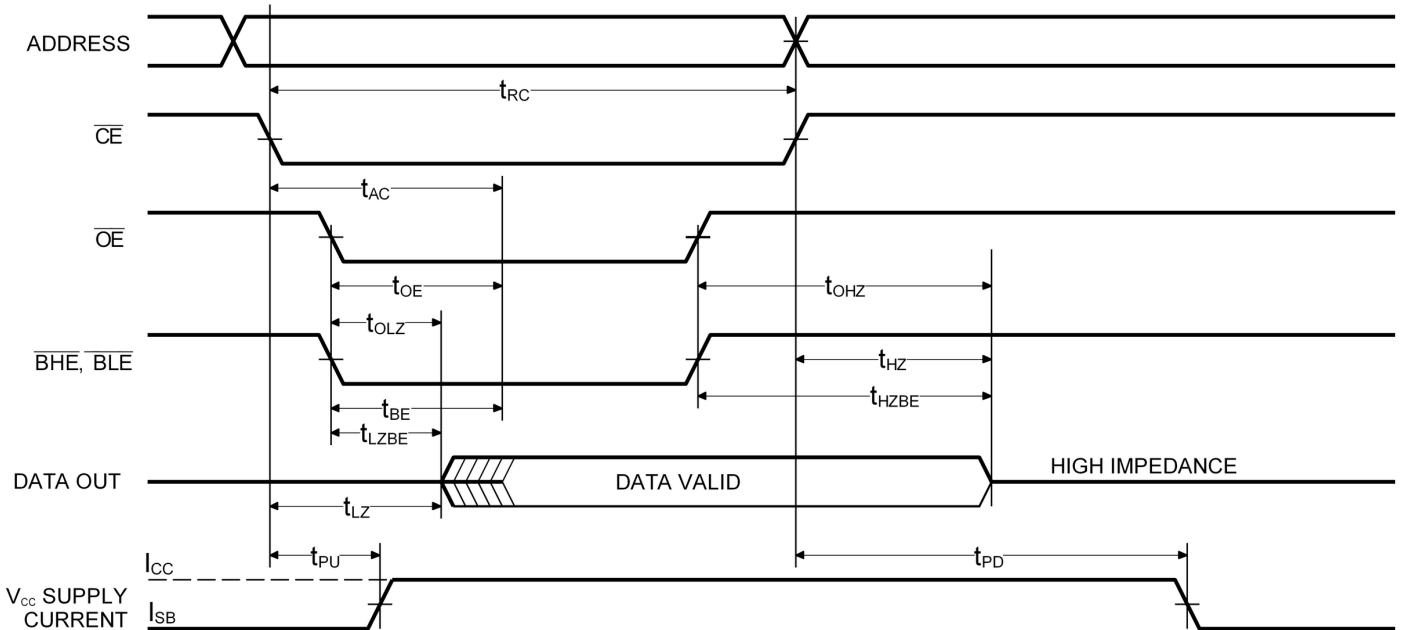
Sym	Parameter	-10		-12		-15		-20		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t <sub>RC</sub>	Read Cycle Time	10		12		15		20		ns
t <sub>AA</sub>	Address Access Time		10		12		15		20	ns
t <sub>AC</sub>	Chip Enable Access Time		10		12		15		20	ns
t <sub>OH</sub>	Output Hold from Address Change	3		3		3		3		ns
t <sub>LZ</sub>	Chip Enable to Output in Low Z	3		3		3		3		ns
t <sub>HZ</sub>	Chip Disable to Output in High Z		5		6		7		8	ns
t <sub>OE</sub>	Output Enable Low to Data Valid		5		7		7		8	ns
t <sub>OLZ</sub>	Output Enable Low to Low Z	0		0		0		0		ns
t <sub>OHZ</sub>	Output Enable High to High Z		5		6		7		8	
t <sub>PU</sub>	Chip Enable to Power Up Time	0		0		0		0		ns
t <sub>PD</sub>	Chip Disable to Power Down Time		10		12		15		20	ns
t <sub>BE</sub>	Byte Enable to Data Valid		5		7		7		8	ns
t <sub>LZBE</sub>	Byte Enable to Low Z	0		0		0		0		ns
t <sub>HZBE</sub>	Byte Disable to High Z		6		6		7		8	ns



## TIMING WAVEFORM OF READ CYCLE NO. 1



## TIMING WAVEFORM OF READ CYCLE NO. 2 ( $\overline{OE}$ CONTROLLED)<sup>(5,6)</sup>



### Notes:

- Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to MAXIMUM rating conditions for extended periods may affect reliability.
- Extended temperature operation guaranteed with 400 linear feet per minute of air flow.
- Transient inputs with  $V_{IL}$  not more negative than  $-2.0V$  and  $V_{IH} \leq V_{CC} + 0.5V$ , are permissible for pulse widths up to 20ns.
- This parameter is sampled and not 100% tested.
- $\overline{WE}$  is HIGH for READ cycle.
- $\overline{CE}$  is LOW and  $\overline{OE}$  is LOW for READ cycle.
- ADDRESS must be valid prior to, or coincident with  $\overline{CE}$  transition LOW.
- Transition is measured  $\pm 200$  mV from steady state voltage prior to change, with loading as specified in Figure 1. This parameter is sampled and not 100% tested.
- Read Cycle Time is measured from the last valid address to the first transitioning address.

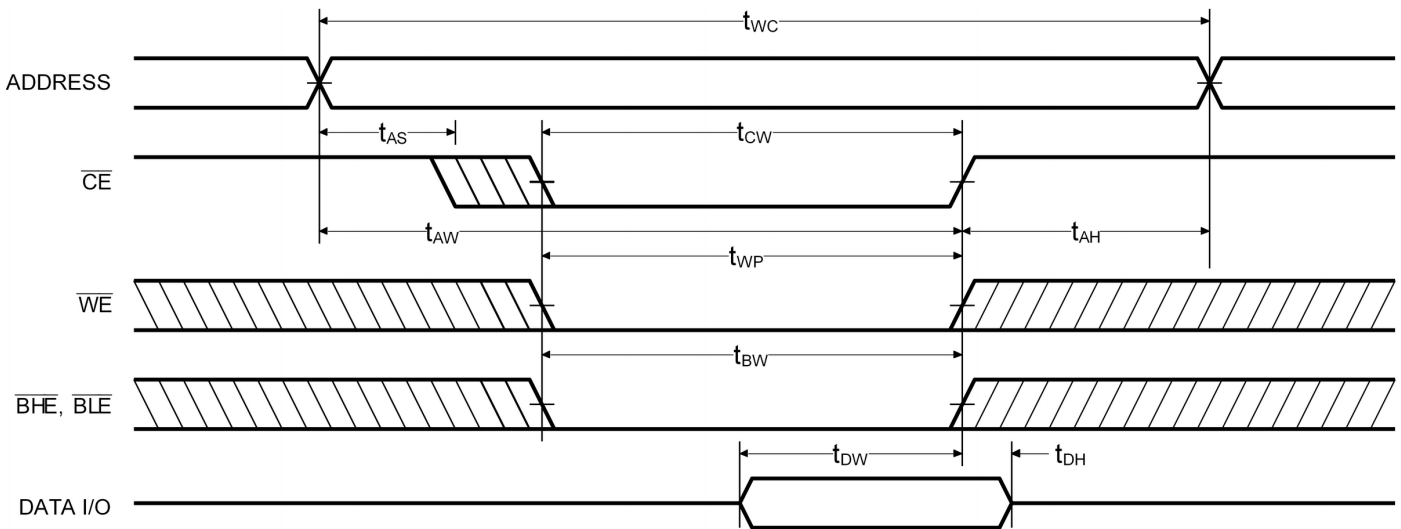


### AC CHARACTERISTICS—WRITE CYCLE

( $V_{CC} = 3.3V \pm 0.3V$ , All Temperature Ranges)<sup>(2)</sup>

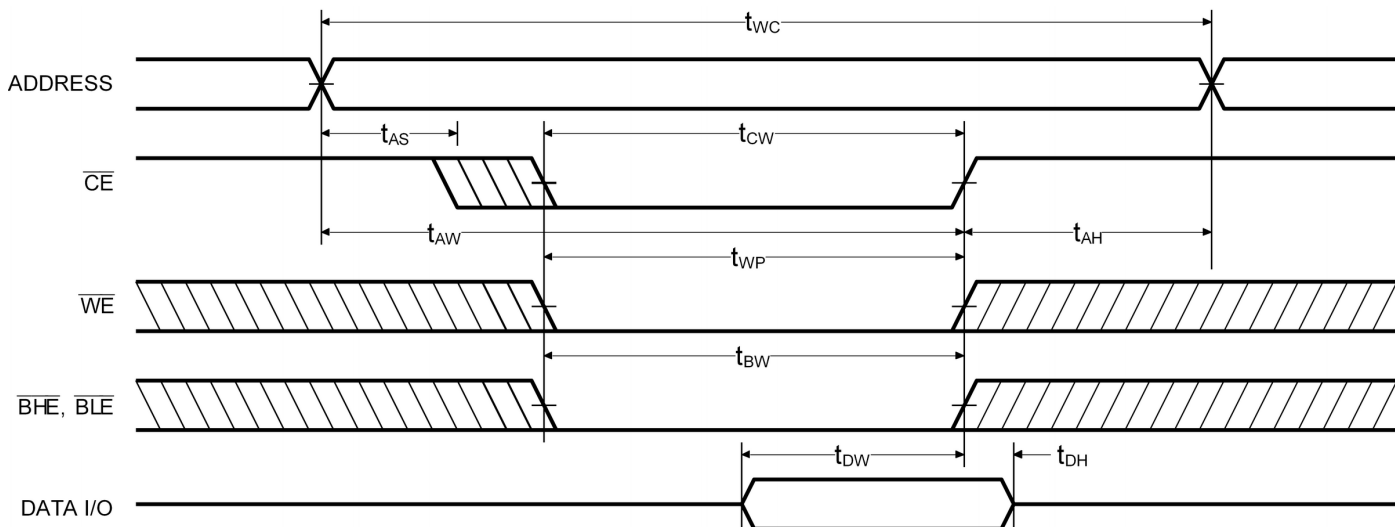
Sym	Parameter	-10		-12		-15		-20		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
$t_{WC}$	Write Cycle Time	10		12		15		20		ns
$t_{CW}$	Chip Enable Time to End of Write	7		8		10		10		ns
$t_{AW}$	Address Valid to End of Write	7		8		10		10		ns
$t_{AS}$	Address Setup Time to Write Start	0		0		0		0		ns
$t_{WP}$	Write Pulse Width	7		8		10		10		ns
$t_{AH}$	Address Hold Time	0		0		0		0		ns
$t_{DW}$	Data Valid to End of Write	5		6		7		8		ns
$t_{DH}$	Data Hold Time	0		0		0		0		ns
$t_{WZ}$	Write Enable to Output in High Z		5		6		7		8	ns
$t_{OW}$	Output Active from End of Write	5		5		0		0		ns
$t_{LZWE}$	$\overline{WE}$ High to Low Z	3		3		3		3		ns
$t_{BW}$	Byte Enable to End of Write	7		8		10		10		ns

### TIMING WAVEFORM OF WRITE CYCLE NO. 1 ( $\overline{CE}$ CONTROLLED)

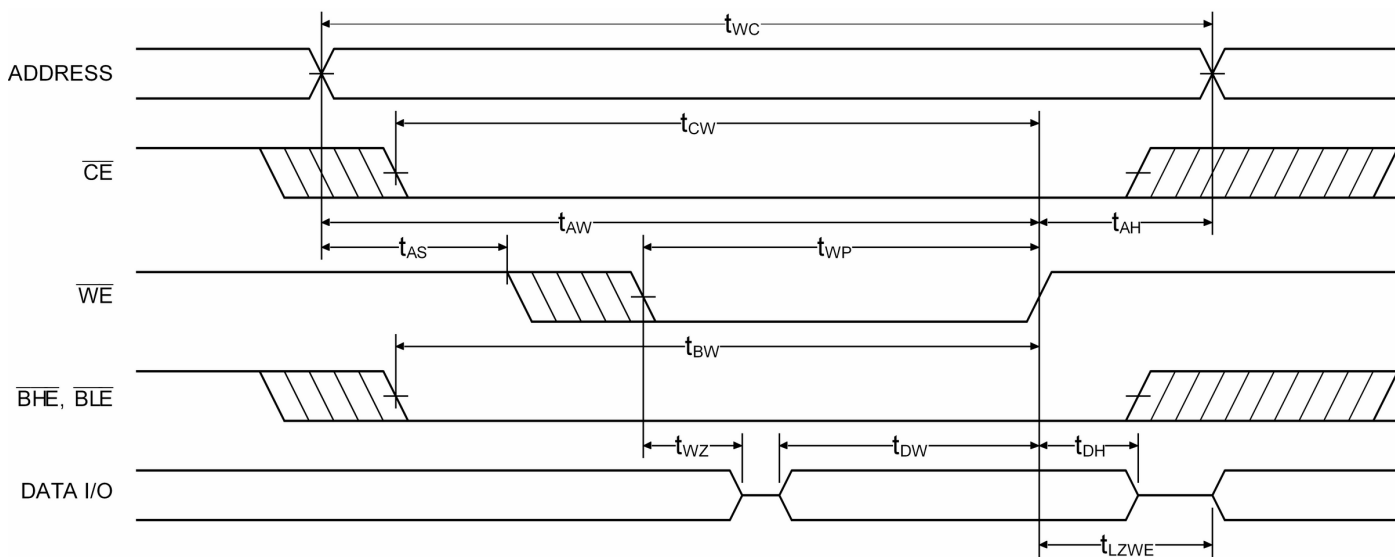




**TIMING WAVEFORM OF WRITE CYCLE NO. 2 ( $\overline{\text{BLE}}$  OR  $\overline{\text{BHE}}$  CONTROLLED)**



**TIMING WAVEFORM OF WRITE CYCLE NO. 3 ( $\overline{\text{WE}}$  CONTROLLED,  $\overline{\text{OE}}$  LOW)**

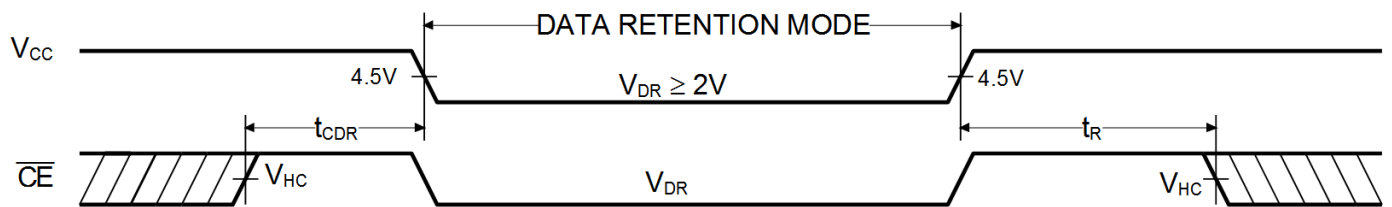




## DATA RETENTION CHARACTERISTICS

Symbol	Parameter	Test Condition	Min	Max	Unit
$V_{DR}$	VCC for Data Retention		2.0		V
$I_{CCDR}$	Data Retention Current	$\overline{CE} \geq V_{CC} - 0.2V,$		10	mA
$t_{CDR}$	Chip Deselect to Data Retention Time	$V_{IN} \geq V_{CC} - 0.2V$ or	0		ns
$t_R^\dagger$	Operation Recovery Time	$V_{IN} \leq 0.2V$	$t_{RC}^\S$		ns

## DATA RETENTION WAVEFORM





### AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns
Input Timing Reference Level	1.5V
Output Timing Reference Level	1.5V
Output Load	See Figures 1, 2, 3

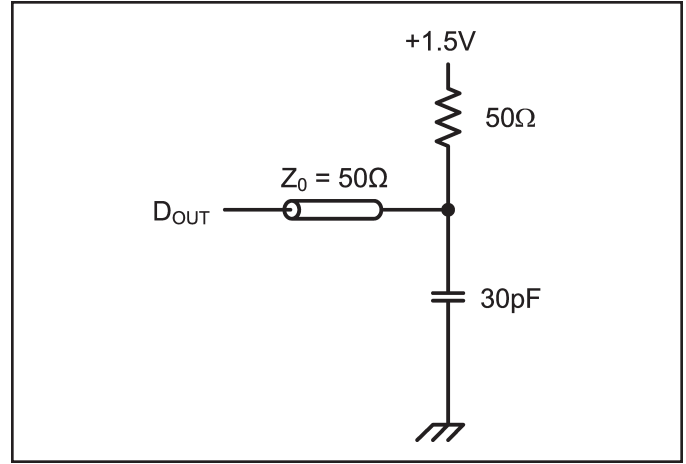


Figure 1. AC Output Load

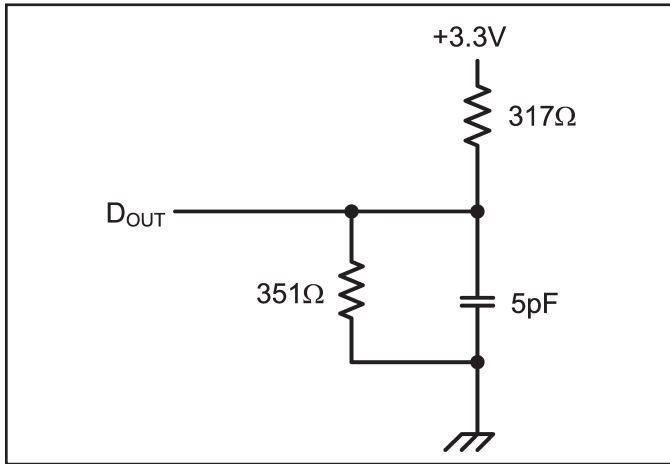


Figure 2. High-Z Output Load

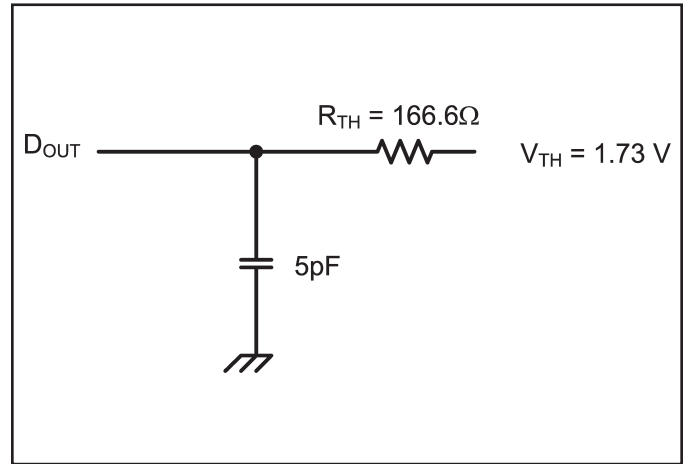


Figure 2. Thevenin Equivalent

\* including scope and test fixture.

**Note:**

Because of the ultra-high speed of the P4C116/L, care must be taken when testing this device; an inadequate setup can cause a normal functioning part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the V<sub>CC</sub> and ground planes

directly up to the contactor fingers. A 0.01 μF high frequency capacitor is also required between V<sub>CC</sub> and ground. To avoid signal reflections, proper termination must be used.

### TRUTH TABLE

Mode	CE	OE	WE	BLE	BHE	I/O <sub>0</sub> -I/O <sub>7</sub>	I/O <sub>8</sub> -I/O <sub>15</sub>	Power
Power-down	H	X	X	X	X	High Z	High Z	Standby
Read All Bits	L	L	H	L	L	D <sub>OUT</sub>	D <sub>OUT</sub>	Active
Read Lower Bits Only	L	L	H	L	H	D <sub>OUT</sub>	High Z	Active
Read Upper Bits Only	L	L	H	H	L	High Z	D <sub>OUT</sub>	Active
Write All Bits	L	X	L	L	L	D <sub>IN</sub>	D <sub>IN</sub>	Active
Write Lower Bits Only	L	X	L	L	H	D <sub>IN</sub>	High Z	Active
Write Upper Bits Only	L	X	L	H	L	High Z	D <sub>IN</sub>	Active
Selected, Outputs Disabled	L	H	H	X	X	High Z	High Z	Active





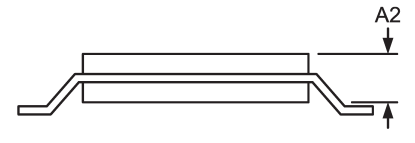
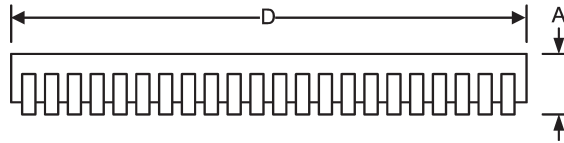
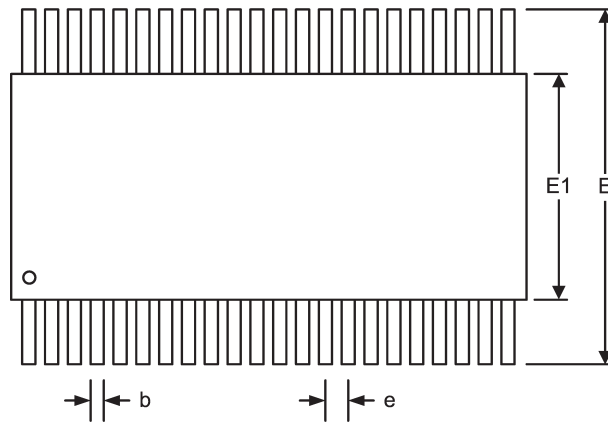
## ORDERING INFORMATION

<u>P3C1041</u>	—	<u>xx</u>	<u>x</u>	<u>x</u>	
Device Type		Speed	Package	Processing	
					C 0°C to +70°C
					I -40°C to +85°C
					T Plastic TSOP II
					10, 12, 15, 20 ns
					256K x 16 SRAM



Pkg #	<b>T2</b>	
# Pins	44	
Symbol	<b>Min</b>	<b>Max</b>
A	0.039	0.047
A <sub>2</sub>	0.033	0.045
b	0.012	0.017
D	0.717	0.733
e	0.0315 BSC	
E	0.453	0.473
E1	0.392	0.408

**TSOP II THIN SMALL OUTLINE PACKAGE**



**REVISIONS**

<b>DOCUMENT NUMBER</b>	SRAM 130
<b>DOCUMENT TITLE</b>	P3C1041 - HIGH SPEED 256K x 16 STATIC CMOS RAM

<b>REV</b>	<b>ISSUE DATE</b>	<b>ORIGINATOR</b>	<b>DESCRIPTION OF CHANGE</b>
OR	Oct-2005	JDB	New Data Sheet
A	Sep-2008	JDB	Updated TSOP II package drawing
B	Sep-2011	JDB	Removed SOJ package