Test Report

for

Single Event Effects Testing

of the

Performance Semiconductor (PACE) 1750A Central Processing Unit

Prepared by

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1.0 Introduction

1.1 Purpose. The purpose of the test was to obtain SEU characterization data on the PACE 1750A CPUs manufactured by Sarnoff for comparison to the original 1750A CPU manufactured by Westinghouse.

1.2 Results Summary. The 1750A CPU manufactured by Sarnoff is acceptable for use in the INU if the process parameters are consistent with either of the two test samples. There are no issues of concern regarding this device type.

1.3 Background. The Aerospace Corporation performed Single Event Effects (SEE) testing on the Performance Semiconductor 1750A Central Processing Unit (CPU) for the Inertial Navigation Unit (INU) program. The testing of the 1750A was deemed necessary because the 1750A CPU design was migrated from Westinghouse to Sarnoff. Ideally, the basic cell structures should be the same as the original PACE CPU. In practice such a statement is not valid, hence testing was needed. The testing was performed by Rocky Koga and Susan Crain of Aerospace on 6/17/98 at the Berkeley 88" Cyclotron SEU Test Facility, which is located at University of California at Berkeley, CA.. Scott Leavy of Honeywell and Jim Elliot of Lockheed Martin witnessed the testing.

2.0 Test Article Descriptions

Two 1750A CPUs were supplied by PACE for SEU testing. These reduced sample sizes were acceptable due to the high cost of each part and the high flip-flop count for each part. A large number of elements tested for each device, in effect, increases the statistical validity of the data. A total of 368 flip-flops were tested in each device. After the testing it was identified that the two 1750A CPUs represented different wafer process parameters, hence the SEU responses were significantly different.

3.0 Test Procedures

The testing was performed using the same test configuration and test software that was used during the testing performed back in 1989 on the 1750A die manufactured by Westinghouse. Since the purpose of this test was to compare the parts manufactured by Sarnoff to the parts manufactured by Westinghouse, duplicating all of the old test procedures and conditions was of prime importance. The parts were tested at room ambient temperature at 5V using Aerospace's BASACS tester. The software exercised the 23 mission critical 16 bit registers with alternating patterns of 5555hex and AAAAhex. In addition, the test exercised an unknown quantity of non-registered logic elements. These circuit elements could be susceptible to transient SEUs that could cause errors in the CPU. These effects were inherently included in the test results since there is no way to mask them out of the SEU data.

4.0 SEU Analysis

4.1 Analysis Method. The piece part test data summarized in paragraph 5.0 was analyzed to determine the predicted SEU rates for each device variety as compared to the old 1750A manufactured by Westinghouse. The summarized data set for each device variety was plotted and fitted to a Weibull distribution. The Weibull parameters were used along with the Space Radiation 4.0 program to calculate the predicted SEU rates for each device. The Space Radiation program was run using the Adam's 90% worst case environment at an inclination of 65 degrees. This orbit is specified in the INU specification. The Adam's 90% worst case terminology means that the cosmic ray environment will be less severe only 10% of the time. This does not account for potentially large fluxes of solar energetic particles that can result from large solar flare events. The total spacecraft and chassis shielding was assumed to be 100 mils of aluminum. This value should represent a nominal, but conservative value. It should be noted that galactic cosmic rays are not easily shielded. For instance, the SEU rates calculated for this report were decreased by less than 10% when the shielding value was increased to 200 mils of aluminum. If this analysis was performed for a device operation during a large solar flare event, shielding would become an issue because solar energetic particles are less penetrating (more easily shielded) than the galactic cosmic rays.

4.2 Weibull Distribution Defined. A Weibull distribution is a mathematical description of the failure behavior in a population of identical components. This distribution has been found to be a reasonable model for describing device failures due to single particles. The Weibull distribution defines the cross-section versus LET curve as a function of four parameters as follows:

$$\sigma(L)=\sigma_{sat}\,[1-\exp(-((L-L_0)/W)^S)]$$

Where σ_{sat} = Asymptotic Saturation Cross-section (cm^2)
L_0 = Absolute LET Threshold (MeV-cm^2/mg)
W = Statistical Width (MeV-cm^2/mg)
s = Statistical Shape

4.3 Notes. It should be noted that the old 1750A SEU test data from 1989 was re-analyzed using the same guidelines so that an accurate SEU rate comparison could be made. The SEU rate calculation methods back in 1989 were not as accurate and tended to be more conservative. In addition, because the old analysis method used could not be understood based on the information available, the current analysis methods were the only way to get an accurate comparison between parts. The final analysis results will be incorporated into the next SEU Analysis update, which is scheduled for submittal later this year.

5.0 Test Results

5.1 Test Data Obtained. During the test the LET vs. cross-section data for the two parts were obtained along with the applicable test configuration and facility beam parameters. This test data is supplied in Appendix A.

5.2 Data Reduction. The SEU data was reduced and plotted to obtain the LET vs. cross-section curve for each data set. The plot for each part was then fitted to a separate Weibull curve. Figures 1 through 3 contain the Weibull curves for the old 1750A CPU, CPU #1 and CPU #2, respectively, along with the data for both test parts and the old 1750A CPU. All of the test data was shown on each curve to allows for an easier comparison from part to part. Table 1 summarizes the Weibull parameters obtained for each data set along with the Figure reference.

Table 1. Test Results Summary

Device	**Saturation Cross-section (cm^2/device)**	**LET Threshold (MeV-cm^2/mg)**	**Weibull Width (MeV-cm^2/mg)**	**Weibull Shape**	**Figure Reference**
Original CPU Data With BASACS	5.00E-6	35.0	37.0	2.0	1
CPU #1 PERF03Z5A 004 1st 3 3	3.77E-6	26.3	57.0	2.1	2
CPU #2 PERF03Z18AAA 001 1st 1 2	3.50E-6	40.0	60.0	3.2	3

5.3 Observations. The CPU #1 device exhibited similar SEU performance as the old 1750A CPU, while the CPU #2 device exhibited significantly better performance. The SEU performance for the two 1750A CPUs tracks the process differences that were supplied by PACE. This is discussed more in paragraph 6.2. From the data obtained it can be assumed that a significant transient SEU problem was not introduced into the design. If a significant transient SEU problem was being exhibited, the CPU #2 data (least responsive test sample) would have been dominated by the transient response.

6.0 Analysis Results

6.1 Results Summary. Once the test data was reduced and the Weibull parameters were defined for each device type, the SEU rates were determined for the Adam's 90% worst case environment for a geosynchronous orbit at an inclination of 65 deg. These SEU results are shown in Table 2, along with all the parameters used to derive the SEU rates. The BASACS testing for the original PACE CPUs was also re-analyzed using the same analysis methods in order to obtain a good comparison of SEU rates. The relative differences between devices are given in the last column in Table 2. The SEU rate for CPU #1 was basically equivalent to the original 1750A CPU even though the Weibull characteristics were slightly different. The SEU rate for CPU #2 was less than the original 1750A CPU by a factor of about 50X.

Table 2. Analysis Results Summary

Device	σ_{sat} (cm^2/ device)	L_0 (MeV-cm^2/mg)	W (MeV-cm^2/mg)	s	Device Depth (μm)	Funnel Length (μm)	SEU Rate (SEU/ device-hr)	Factor vs. Original
Original CPU Data With BASACS	5.00E-6	35.0	37.0	2.0	0.5	0.0	1.13E-9	--
CPU #1 PERF03Z5A 004 1st 3 3	3.77E-6	26.3	57.0	2.1	0.5	0.0	6.37E-10	0.56
CPU #2 PERF03Z18AAA 001 1st 1 2	3.50E-6	40.0	60.0	3.2	0.5	0.0	1.89E-11	0.017

6.2 Correlation to Design and Process Information. After the testing was completed, it was found out from PACE that the two 1750A CPU devices were from two different wafer lots that had slightly different process parameters. The process differences appear to qualitatively explain the different SEU responses between CPU #1 and CPU #2 (and in part the original CPU). CPU #1 had a gate oxide thickness of 280Å and CPU #2 had a gate oxide thickness of 230Å. Based on old hardcopy data, the original CPU had a gate oxide thickness of 250Å. The gate oxide thickness is inversely proportional to the gate capacitance. The gate capacitance in turn is proportional to the critical charge and hence the LET threshold of the device. Based on these relationships it should be expected that a larger gate oxide thickness (holding everything else constant) would give a lower LET threshold due to a decreased gate capacitance. This is demonstrated by the fact that CPU #1 had the largest gate oxide thickness and the lowest LET threshold, while CPU #2 had the smallest gate oxide thickness and the highest LET threshold. The devices also had different L_{eff} (channel length) values. CPU #1 had an L_{eff} of 0.904μm and CPU #2 had an L_{eff} of 1.025μm. A higher L_{eff} value should result in a larger gate area. The increased gate area gives a higher critical charge and thus less sensitivity to SEU. Since the channel sizes were not greatly different the saturation cross-section should not have been affected to large extent. The data shows that the saturation cross-sections were approximately the same for CPU #1 and CPU #2. The L_{eff} of the original CPU was not found, so no comparison is made.

7.0 Conclusions and Recommendations

Based on the test and analysis results, the 1750A CPU device fabricated by Sarnoff is acceptable for use in the INU FCSP and IMSP assemblies. Either set of process parameters are acceptable. Both test samples displayed an SEU rate of less than the original 1750A manufactured by Westinghouse. The flight devices should be manufactured with the same process parameters used to fabricate the test articles. No latchup was observed and no SEU transient mechanism was exhibited.

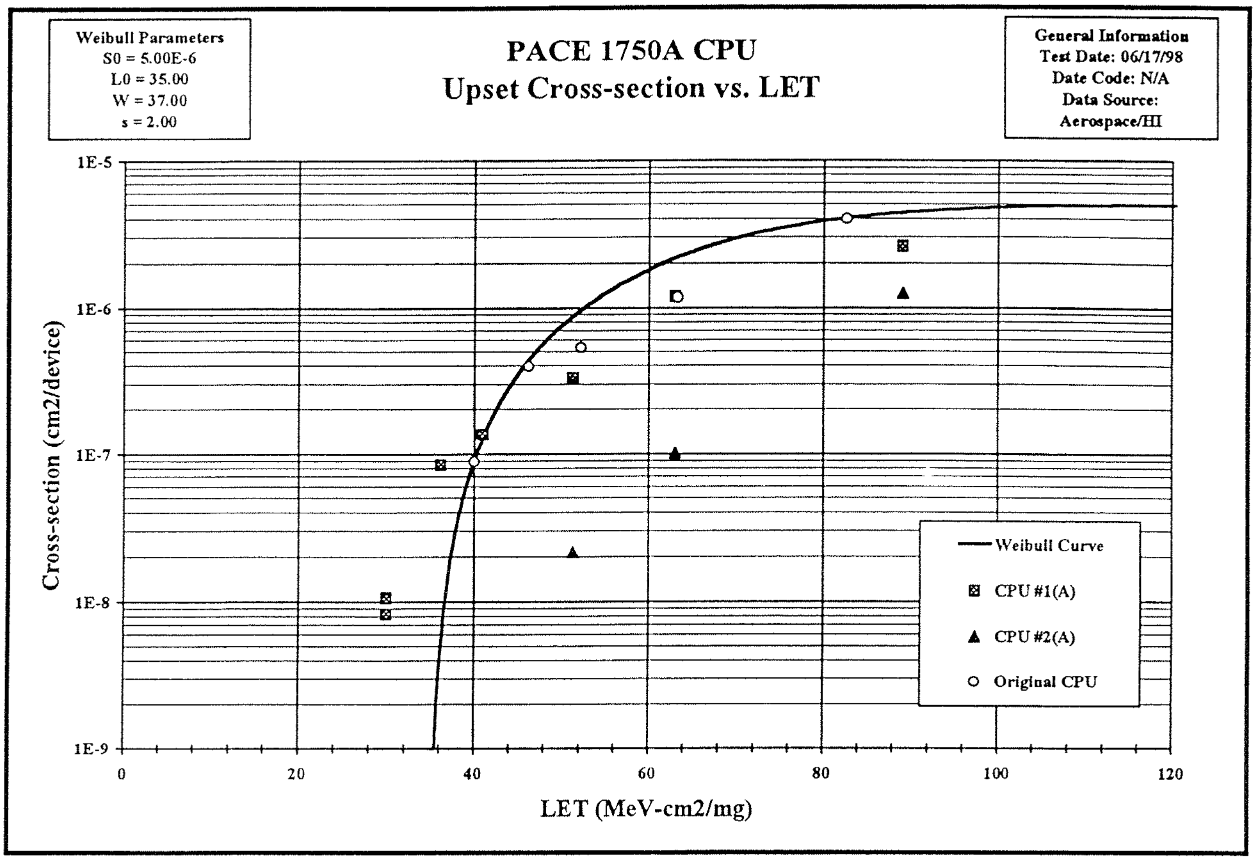

Figure 1. Weibull Curve Fit for the Original CPU

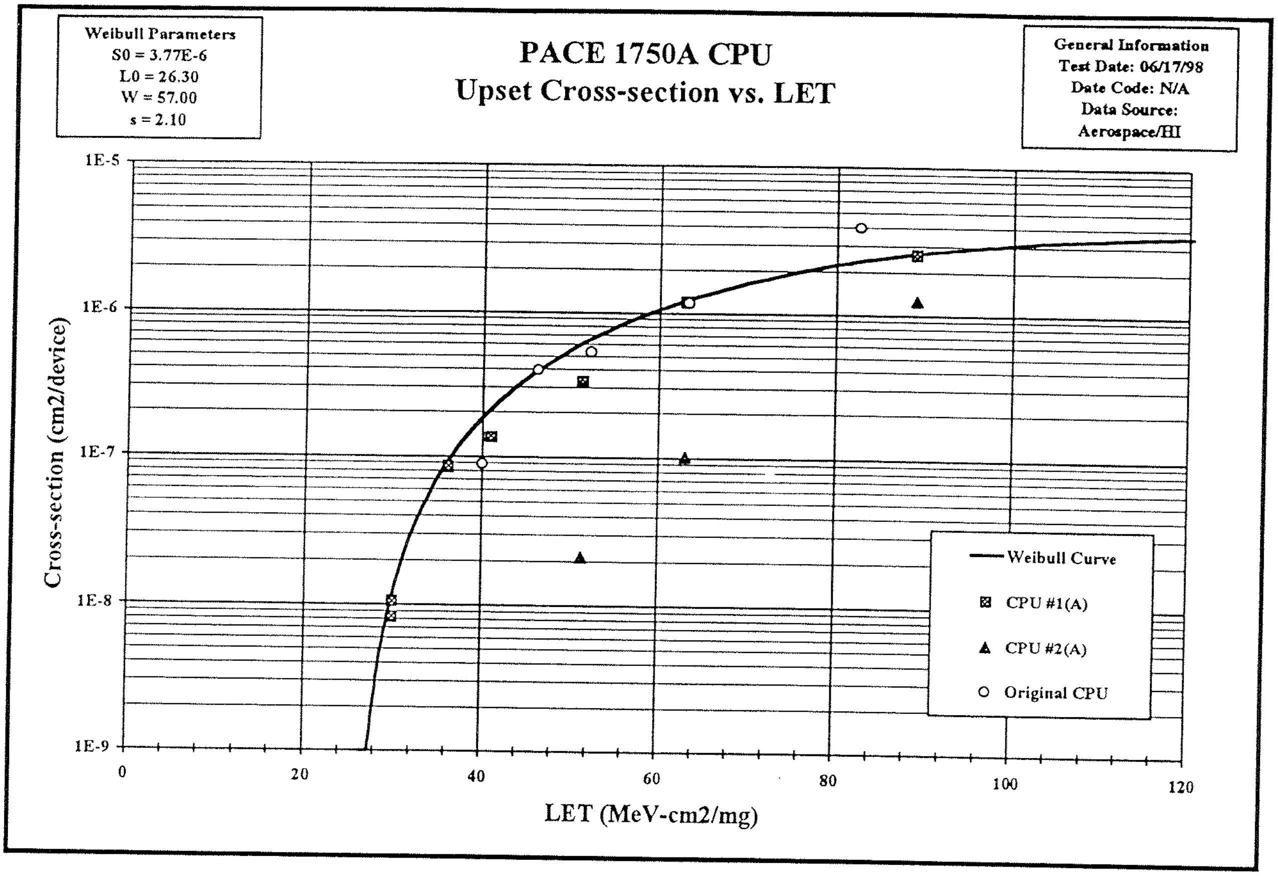

Figure 2. Weibull Curve Fit for CPU #1

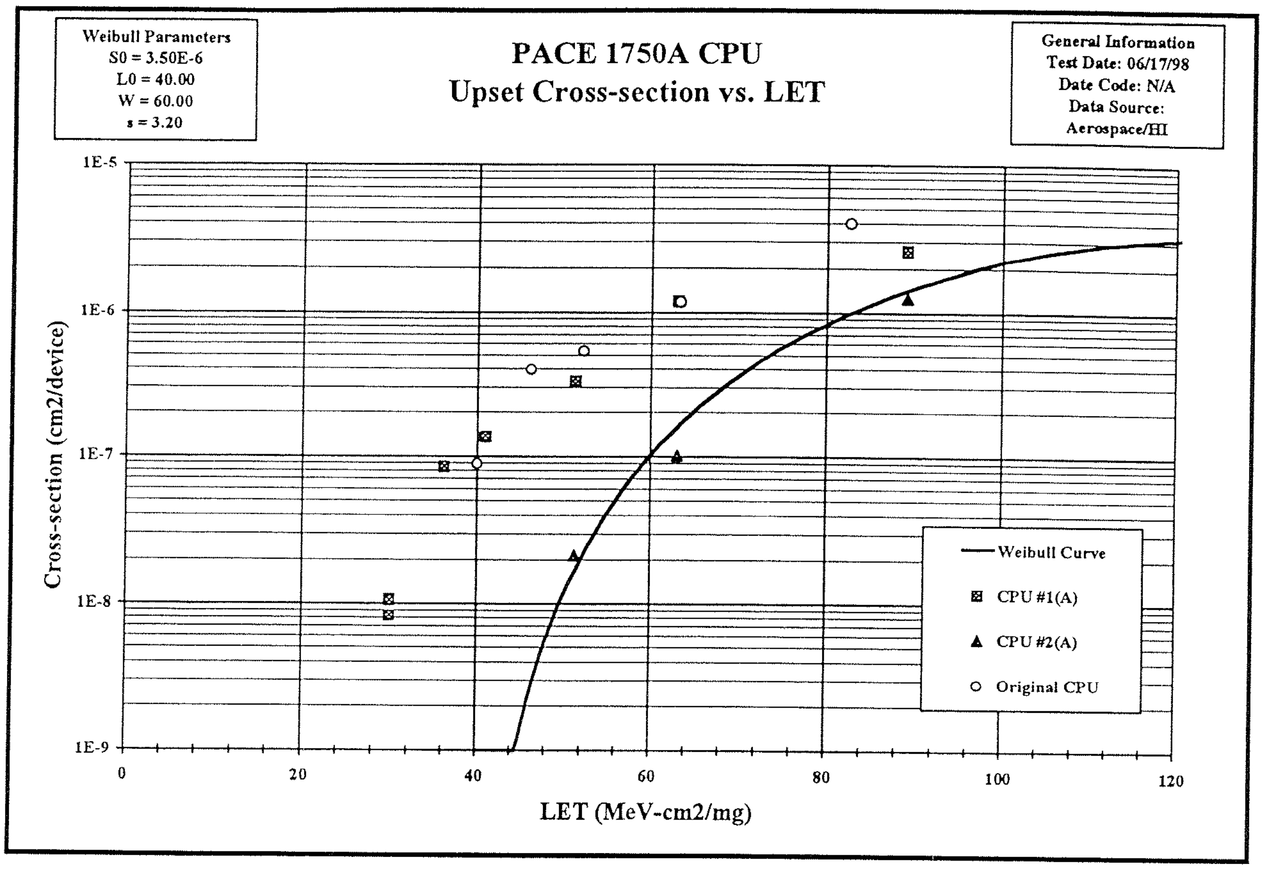

Figure 3. Weibull Curve Fit for CPU #2