PYRAMID SEMICONDUCTOR CORPORATION

PYA28C040A

128K X 32 EEPROM MODULE

FEATURES

- **Access Times of 120, 150, 200, and 250 ns**
- **Single 5V±10% Power Supply**
- **Simple Byte and Page Write**
- **Low Power CMOS:**
  - **60 mA Active Current**
  - **500 µA Standby Current**
- **Organized as 128K x32; User configurable as 256K x16 or 512K x8**
- **Built in decoupling caps for low noise operation**
- **Fast Write Cycle Times**
- **Software Data Protection**
- **Fully TTL Compatible Inputs and Outputs**
- **Endurance:**
  - **10,000 Cycles/byte**
  - **100,000 Cycles/page**
- **Data Retention: 100 Years**
- **Available in the following package:**
  - **68-Pin QFP**

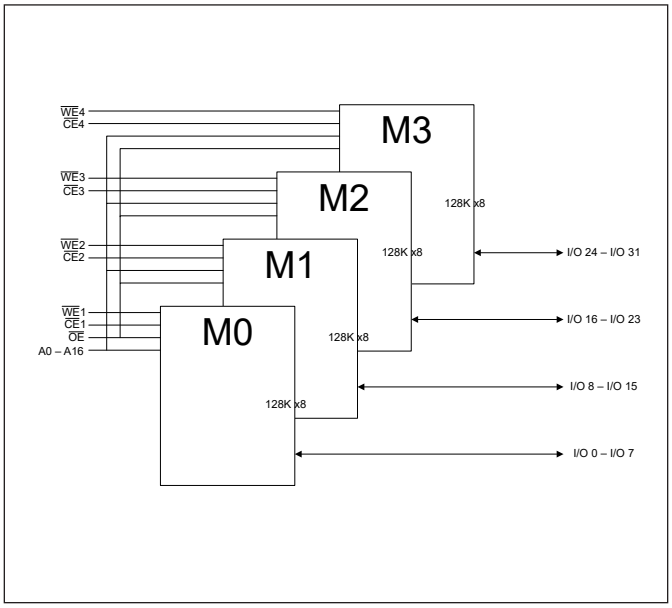
DESCRIPTION

The Pyramid Semiconductor Corp. PYA28C040A is a 4 Megabit EEPROM Module organized as 128K x 32 bit and is user configurable to 256K x 16 or 512K x 8. The module achieves high speed access, low power consumption and high reliability by employing advanced CMOS memory technology.

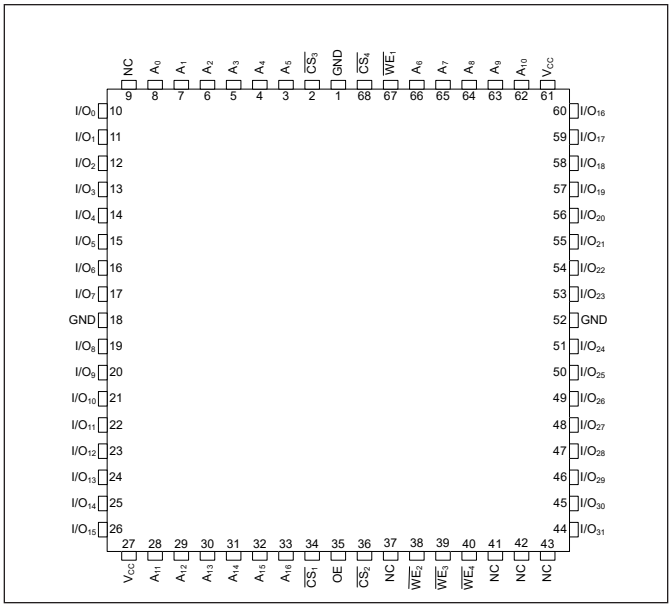
This memory module is manufactured in compliance to the MIL-STD 883, making the PYA28C040A ideally matched for military or space applications.

The module is offered as a 68 lead 0.990 inch square ceramic quad flat pack. It has a max height of 0.200 inch. This package design is targeted for applications which require low profile SMT packaging.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



OPERATION

DEVICE OPERATION

The 128K x 32 EEPROM memory solution is an electrically erasable and programmable memory module that is accessed like a Static RAM for the read or write cycle without the need for external components. The device contains a 128-byte-page register to allow writing of up to 128 bytes of data simultaneously. During a write cycle, the address and 1 to 128 bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by DATA polling of I/O_7. Once the end of a write cycle has been detected a new access for a read or write can begin.

READ

The memory module is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is High, the data stored at the memory location determined by the address pins is asserted on the outputs. The module can be read as a 32 bit, 16 bit or 8 bit device. The outputs are put in the high impedance state when either $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention in their system.

BYTE WRITE

A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high initiates a write cycle. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Once a BWDW (byte, word or double word) write has been started it will automatically time itself to completion.

PAGE WRITE

The page write operation of the 128K x 32 EEPROM allows 1 to 128 BWDWs of data to be written into the device during a single internal programming period. Each new BWDW must be written within 150 µs (t_{BLC}) of the previous BWDW. If the t_{BLC} limit is exceeded, the memory module will cease accepting data and commence the internal programming operation. For each WE high to low transition during the page write operation, A_7-A_{16} must be the same.

The A_0-A_6 inputs are used to specify which bytes within the page are to be written. The bytes may be loaded in any order and may be altered within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

DATA POLLING

This memory module features DATA Polling to indicate the end of a write cycle. During a byte or page write cycle, an attempted read of the last byte written will result in the complement of the written data to be presented on I/O_7. Once the write cycle has been completed, true data is valid on all outputs, and the next write cycle may begin. DATA Polling may begin at anytime during the write cycle.

TOGGLE BIT

In addition to DATA Polling the module provides another method for determining the end of a write cycle. During the write operation, successive attempts to read data from the device will result in I/O_6 of the accessed die toggling between one and zero. Once the write has completed, I/O_6 will stop toggling and valid data will be read. Reading the toggle bit may begin at any time during the write cycle.

DATA PROTECTION

Pyramid Semiconductor has incorporated both hardware and software features that will protect the memory against inadvertent writes during transitions of the host system power supply.

HARDWARE PROTECTION

Hardware features protect against inadvertent writes to the PYA28C040A in the following ways: (a) V_{CC} sense - if V_{CC} is below 3.8 V (typical) the write function is inhibited; (b) V_{CC} power-on delay - once V_{CC} has reached 3.8 V the device will automatically time out 5 ms (typical) before allowing a write; (c) write inhibit - holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits write cycles; (d) noise filter - pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a write cycle.

SOFTWARE DATA PROTECTION

A software controlled data protection feature has been implemented on the PYA28C040A. When enabled, the software data protection (SDP), will prevent inadvertent writes. The SDP feature may be enabled or disabled by the user; the PYA28C040A is shipped from Pyramid Semiconductor with SDP disabled.

SDP is enabled by the host system issuing a series of three write commands; three specific bytes of data are written to three specific addresses (refer to Software Data Protection Algorithm). After writing the 3-byte command sequence and after t_{WC} the entire PYA28C040A will be protected against inadvertent write operations. It should be noted, that once protected the host may still perform a byte or page write to the PYA28C040A. This is done by preceding the data to be written by the same 3-byte command sequence used to enable SDP.

Once set, SDP will remain active unless the disable command sequence is issued. Power transitions do not disable SDP and SDP will protect the PYA28C040A during power-up and power-down conditions. All command sequences must conform to the page write timing specifications. The data in the enable and disable command sequences is not written to the device and the memory addresses used in the sequence may be written with data in either a byte or page write operation.

After setting SDP, any attempt to write to the device without the 3-byte command sequence will start the internal write timers. No data will be written to the device; however, for the duration of t_{WC}, read operations will effectively be polling operations.

DEVICE IDENTIFICATION

An extra 128-bytes of EEPROM memory are available on each die to the user for device identification. By raising A_9 to 12 V ± 0.5 V and using address locations 1FF80H to 1FFFFH the bytes may be written to or read from in the same manner as the regular memory array.

MAXIMUM RATINGS[1]

Sym	Parameter	Value	Unit
V_{CC}	Power Supply Pin with Respect to GND	-0.3 to +6.25	V
V_{TERM}	Terminal Voltage with Respect to GND (up to 6.25 V)	-0.5 to +6.25	V
T_A	Operating Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Grade[2]	Ambient Temp	GND	V_{CC}
Military	-55 °C to +125 °C	0V	5.0 V ± 10%

CAPACITANCES[4]

(V_{CC} = 5.0 V, T_A = 25 °C, f = 1.0 MHz)

Sym	Parameter	Conditions	Typ	Unit
C_{ADD}	A_0 - A_{16} Capacitance	V_{IN} = 0 V	40	pF
C_{OE}	$\overline{OE}$ Capacitance	V_{IN} = 0 V	40	pF
C_{WCE}	$\overline{WE}$ and $\overline{CE}$ Capacitance	V_{IN} = 0 V	10	pF
C_{IO}	I/O_0 - I/O_{31} Capacitance	V_{OUT} = 0 V	12	pF

DC ELECTRICAL CHARACTERISTICS

(Over Recommended Operating Temperature & Supply Voltage)[2]

Sym	Parameter	Test Conditions	PYA28C040A		Unit
			Min	Max	
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.3	V
V_{IL}	Input Low Voltage		-0.5[3]	0.8	V
V_{HC}	CMOS Input High Voltage		V_{CC} - 0.2	V_{CC} + 0.5	V
V_{LC}	CMOS Input Low Voltage		-0.5[3]	0.2	V
V_{OL}	Output Low Voltage (TTL Load)	I_{OL} = +2.1 mA, V_{CC} = Min		0.45	V
V_{OH}	Output High Voltage (TTL Load)	I_{OH} = -0.4 mA, V_{CC} = Min	2.4		V
I_{LI}	Input Leakage Current	V_{CC} = Max V_{IN} = GND to V_{CC}	-10	+10	µA
I_{LO}	Output Leakage Current	V_{CC} = Max, $\overline{CE}$ = V_{IH}, V_{OUT} = GND to V_{CC}	-10	+10	µA
I_{SBT1}	Standby Power Supply Current	$\overline{CE}$ ≥ V_{IH}, V_{CC} = Max, f = 0 Hz, All Other inputs ≤ V_{IL} or ≥ V_{IH}	—	15	mA
I_{SBT2}	Standby Power Supply Current	$\overline{CE}$ ≥ V_{CC} - 0.2 V, V_{CC} = Max, f = 0 Hz, V_{IL} ≤ V_{SS} +0.2 V or V_{IH} ≥ V_{CC} - 0.2 V	—	1	mA
I_{SBT3}	Standby Power Supply Current	$\overline{CE}$ = V_{CC}, $\overline{OE}$ = V_{IH} , V_{CC} = 5.5 Vdc, A_0 - A_{16} change at 5 MHz, CMOS levels	—	5	mA
I_{CC}	Supply Current	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}, Outputs Open, Inputs = V_{CC} = 5.5 V	—	250	mA

Notes:

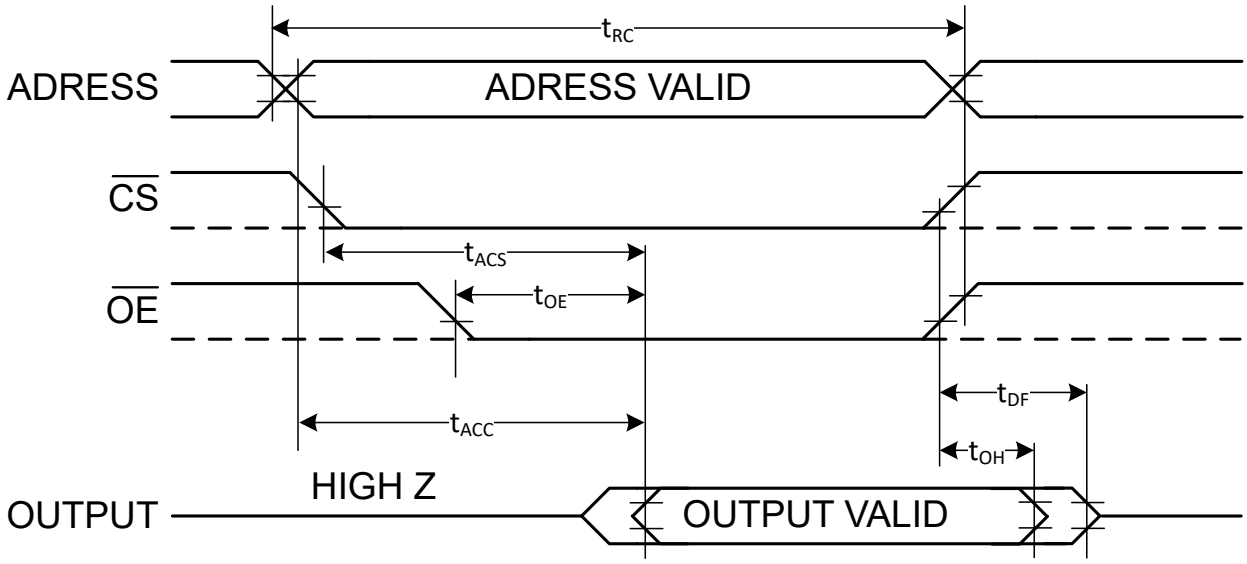
1. Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to MAXIMUM rating conditions for extended periods may affect reliability.
2. Extended temperature operation guaranteed with 400 linear feet per minute of air flow.
3. Transient inputs with V_{IL} and I_{IL} not more negative than -3.0 V and -100 mA, respectively, are permissible for pulse widths up to 20 ns.
4. This parameter is sampled and not 100% tested.

AC ELECTRICAL CHARACTERISTICS — READ CYCLE

(V_{CC} = 5V ± 10%, All Temperature Ranges)[2]

Sym	Parameter	-120		-150		-200		-250		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{RC}	Address to Output Delay	120		150		200		250		ns
t_{ACC}	Address to Output Delay		120		150		200		250	ns
t_{ACS}	Address Access Time		120		150		200		250	ns
t_{OE}	$\overline{OE}$ to Output Delay	0	50	0	55	0	55	0	55	ns
t_{DF}	$\overline{OE}$ or $\overline{CE}$ to Output Float		55		55		55		55	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address Change	0		0		0		0		ns

TIMING WAVEFORM OF READ CYCLE



AC ELECTRICAL CHARACTERISTICS — WRITE CYCLE

(V_{CC} = 5V ± 10%, All Temperature Ranges)[2]

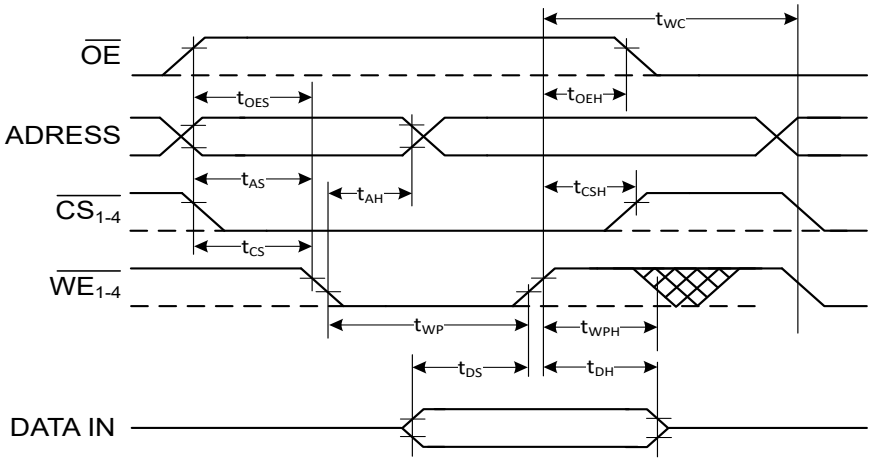
Sym	Parameter	Min	Max	Unit
t_{WC}	Write Cycle Time (Typ. is 6 ms)		10	ms
t_{AS}	Address Set-up Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CS}$)	100		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{AH}	Address Hold Time	100		ns
t_{DH}	Data Hold Time	10		ns
t_{CSH}	Chip Select Hold Time	0		ns
t_{DS}	Data Set-up Time	50		ns
t_{OES}	Output Enable Set-up Time	0		ns
t_{OEH}	Output Enable Hold Time	0		ns
t_{WPH}	Write Pulse Width High	50		ns

WRITE CYCLE TIMING

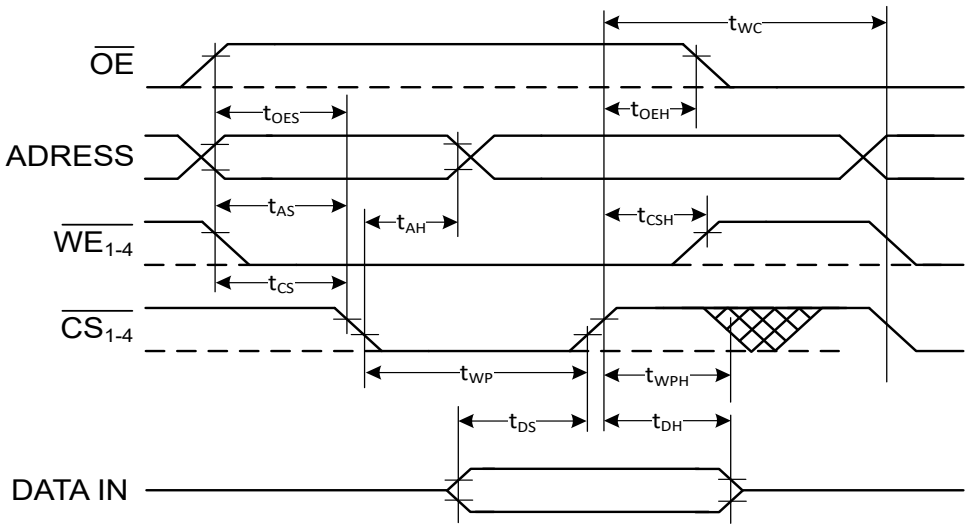
Figures below show the write cycle timing relationships. A write cycle begins with address application, write enable and chip select. Chip select is accomplished by placing the $\overline{CS}$ signal low. Write enable consists of setting the $\overline{WE}$ signal low. The write cycle begins when the last of either $\overline{CS}$ or $\overline{WE}$ goes low.

The WE line transition from high to low also initiates an internal 150 µs delay timer to permit page mode operation. Each subsequent $\overline{WE}$ transition from high to low that occurs before the completion of the 150 µs time out will restart the timer from zero. The operation of the timer is the same as a retriggerable one-shot.

TIMING WAVEFORM OF WRITE CYCLE $\overline{WE}$ CONTROLLED



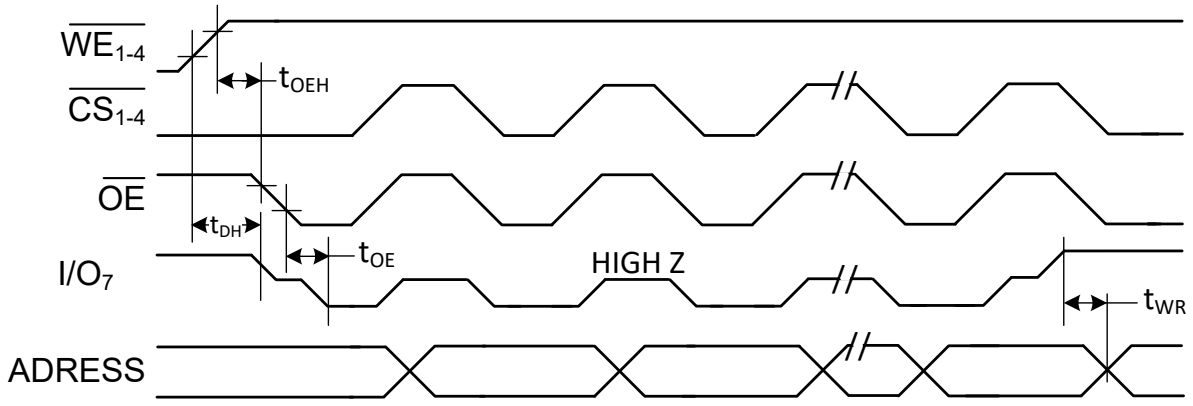
TIMING WAVEFORM OF WRITE CYCLE $\overline{CS}$ CONTROLLED



DATA POLLING

The PYA28C040A offers a data polling feature which allows a faster method of writing to the device. The figure below shows the timing diagram for this function. During a byte or page write cycle, an attempted read of the last byte written will result in the complement of the written data on D_7 (for each chip). Once the write cycle has been completed, true data is valid on all outputs and the next cycle may begin. Data polling may begin at any time during the write cycle.

Sym	Parameter	Min	Max	Unit
t_{DH}	Data Hold Time	10		ns
t_{OEH}	$\overline{OE}$ Hold Time	10		ns
t_{OE}	$\overline{OE}$ To Output Valid		55	ns
t_{WR}	Write Recovery Time	0		ns

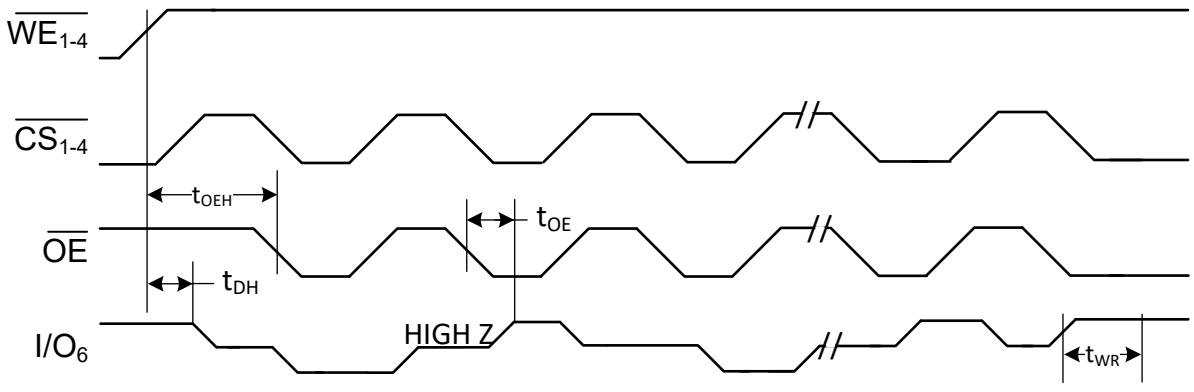


TOGGLE BIT(1,2)

In addition to DATA polling, another method for determining the end of a write cycle is provided. During the write operation, successive attempts to read data from the device will result in I/O_6 toggling between one and zero. Once the write has completed, I/O_6 will stop toggling and valid data will be read. Reading the toggle bit may begin at any time during the write cycle.

Sym	Parameter	Min	Max	Unit
t_{DH}	Data Hold Time	10		ns
t_{OEH}	$\overline{OE}$ Hold Time	10		ns
t_{OE}	$\overline{OE}$ To Output Valid(3)			ns
t_{OEHP}	$\overline{OE}$ High pulse	150		ns
t_{WR}	Write Recovery Time	0		ns

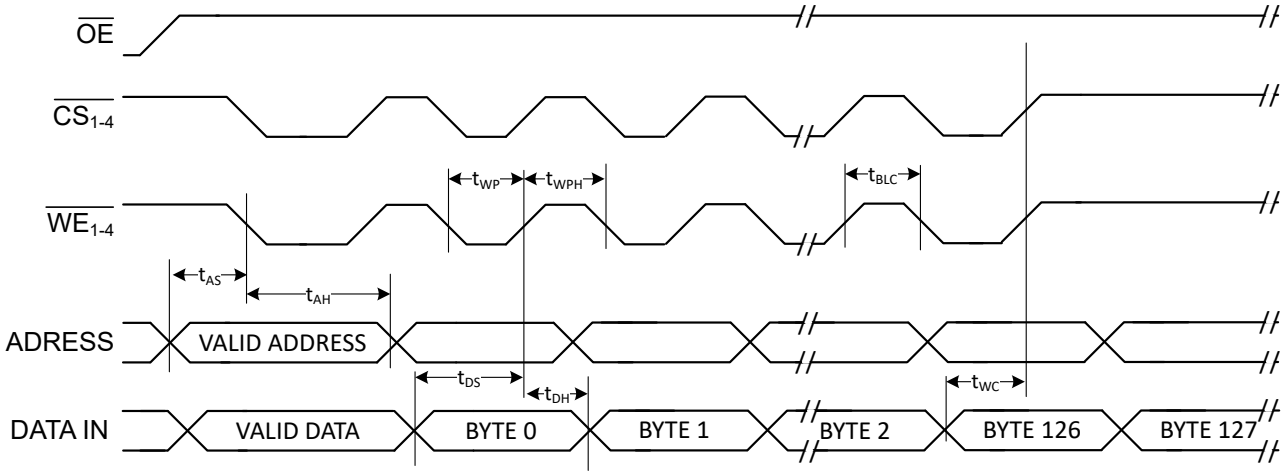
Notes:
1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
2. Any address location may be used but the address should not vary.
3. Beginning and ending state of I/O_6 will vary.



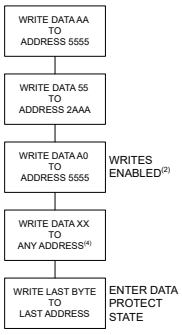
PAGE WRITE CHARACTERISTICS

(V_{CC} = 5V ± 10%, All Temperature Ranges)

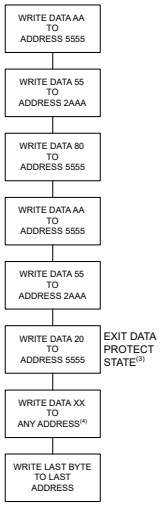
Sym	Parameter	Min	Max	Unit
t_{WC}	Write Cycle Time (Typ. is 6 ms)		10	ms
t_{AS}	Address Set-up Time	0		ns
t_{AH}	Address Hold Time(1)	100		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}	Data Hold Time	10		ns
t_{WP}	Write Pulse Width	100		ns
t_{BLC}	Byte Load Cycle Time		150	µs
t_{WPH}	Write Pulse Width High	50		ns



SOFTWARE DATA PROTECTION ENABLE ALGORITHM



SOFTWARE DATA PROTECTION DISABLE ALGORITHM



Notes:

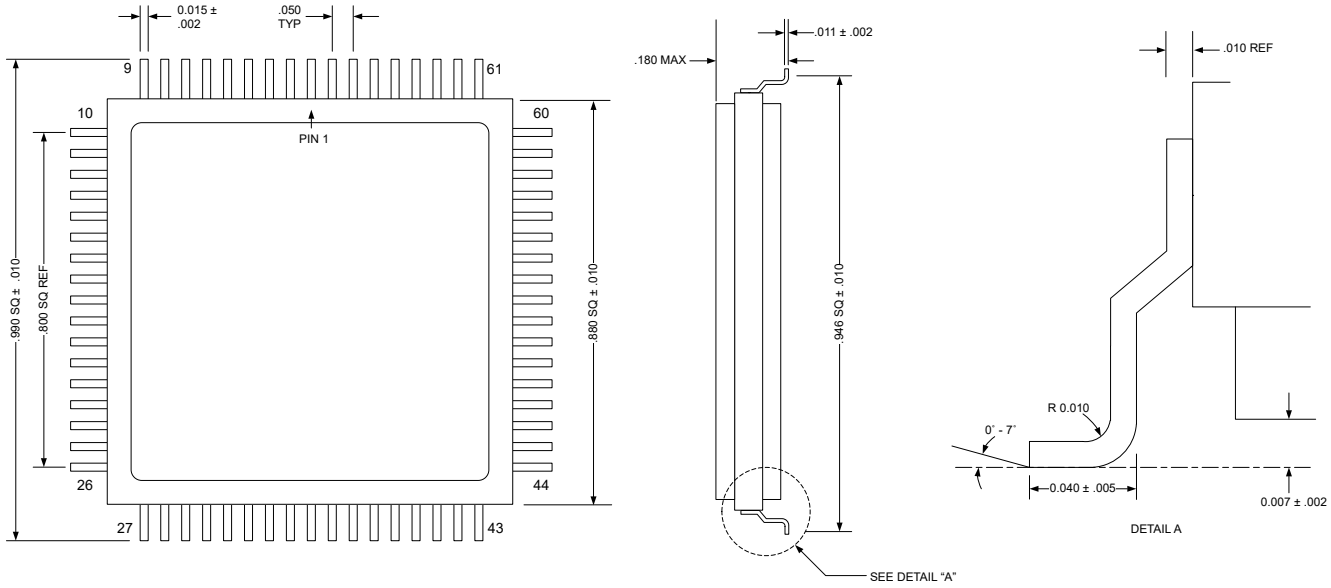
1. Data format: I/O_7 - I/O_0 (Hex) , Address format: A_{16} - A_0 (Hex)
2. Write protect state will be active at end of write even if no data is loaded.
3. Write Protect state will be deactivated at end of period even if no other data is loaded.
4. 1 to 128 bytes of data are loaded.

ORDERING INFORMATION

PYA28C040A — xx — x — x

	Device Type	Speed	Package	Processing
	128K x 32 EEPROM	12, 15, 20, 25 (12 = 120 ns, etc.)	QG 68-Pin Ceramic QFP Gullwing, 880 x 880 mil	M -55°C to +125°C MB Test Method 5004 Process

QFP GULLWING



REVISIONS

DOCUMENT NUMBER	PYA28C040
DOCUMENT TITLE	PYA28C040A - 128K x 32 EEPROM

REV	ISSUE DATE	ORIGINATOR	DESCRIPTION OF CHANGE
OR	Dec 2025	VM	New Data Sheet